UNIT-1 BIASING OF DISCRETE BJT AND MOSFET

DC LOAD LINE AND OPERATING POINT

For the transistor to properly operate it must be biased. There are several methods to establish the DC operating point. We will discuss some of the methods used for biasing transistors as well as troubleshooting methods used for transistor bias circuits.

The goal of amplification in most cases is to increase the amplitude of an ac signal without altering it.

Biasing in electronics is the method of establishing predetermined voltages or currents at various points of an electronic circuit for the purpose of establishing proper operating conditions in electronic components. Many electronic devices whose function is signal processing time-varying (AC) signals also require a steady (DC) current or voltage to operate correctly. The AC signal applied to them is superposed on this DC bias current or voltage. Other types of devices, for example magnetic recording heads, require a time-varying (AC) signal as bias. The operating point of a device, also known as bias point, quiescent point, or Q-point, is the steady-state voltage or current at a specified terminal of an active device (a transistor or vacuum tube) with no input signal applied

Most often, bias simply refers to a fixed DC voltage applied to the same point in a circuit as an alternating current (AC) signal, frequently to select the desired operating response of a semiconductor or other electronic component (forward or reverse bias). For example, a bias voltage is applied to a transistor in an electronic amplifier to allow the transistor to operate in a particular region of its transconductance curve. For vacuum tubes, a (much higher) grid bias voltage is also often applied to the grid electrodes for precisely the same reason.

A hot bias can lower the tube life span, but a "cool" bias can induce crossover distortion.

Bias is also the term used for a high-frequency signal added to the audio signal recorded on magnetic tape. See tape bias.

Bias is used in direct broadcast satellites such as DirecTV and Dish Network, the integrated receiver/decoder (IRD) box actually powers the feedhorn or low-noise block converter (LNB) receiver mounted on the dish arm. This bias is changed from a lower voltage to a higher voltage to select the polarization of the LNB, so that it receives signals that are polarized either horizontal or vertical, thereby allowing it to receive twice as many channels.

We still need to determine the optimal values for the DC biasing in order to choose resistors, etc. This bias point is called the quiescent or Q-point as it gives the values of the voltages when no input signal is applied. To determine the Q-point we need to look at the range of values for which the transistor is in the active region.

Bipolar junction transistors

For bipolar junction transistors the bias point is chosen to keep the transistor operating in the active mode, using a variety of circuit techniques, establishing the Q-point DC voltage and current. A small signal is then applied on top of the Q-point bias voltage, thereby either modulating or switching the current, depending on the purpose of the circuit.

The quiescent point of operation is typically near the middle of the DC load line. The process of obtaining a certain DC collector current at a certain DC collector voltage by setting up the operating point is called biasing.

After establishing the operating point, when an input signal is applied, the output signal should not move the transistor either to saturation or to cut-off. However, this unwanted shift still might occur, due to the following reasons:

1. Parameters of transistors depend on junction temperature. As junction temperature increases, leakage current due to minority charge carriers (I_{CBO}) increases. As I_{CBO} increases, I_{CEO} also

increases, causing an increase in collector current I_C. This produces heat at the collector junction. This process repeats, and, finally, the Q-point may shift into the saturation region. Sometimes, the excess heat produced at the junction may even burn the transistor. This is known as thermal runaway.
2. When a transistor is replaced by another of the same type, the Q-point may shift, due to changes in parameters of the transistor, such as current gain (β) which varies slightly for each unique transistor.

To avoid a shift of Q-point, bias-stabilization is necessary. Various biasing circuits can be used for this purpose.

Load line

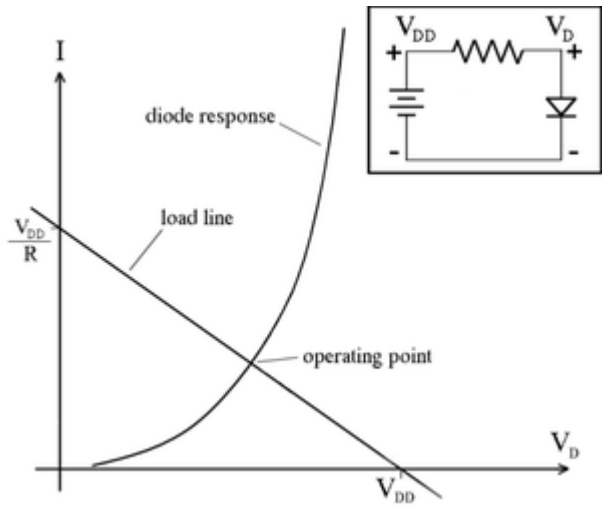
A **load line** is used in graphical analysis of nonlinear electronic circuits, representing the constraint other parts of the circuit place on a non-linear device, like a diode or transistor. It is usually drawn on a graph of the current vs the voltage in the nonlinear device, called the device's characteristic curve. A load line, usually a straight line, represents the response of the linear part of the circuit, connected to the nonlinear device in question. The operating point(s) of the circuit are the points where the characteristic curve and the load line intersect; at these points the current and voltage parameters of both parts of the circuit match.[1]

The example at right shows how a load line is used to determine the current and voltage in a simple diode circuit. The diode, a nonlinear device, is in series with a linear circuit consisting of a resistor, R and a voltage source, V_{DD}. The characteristic curve (curved line), representing current I through the diode versus voltage across the diode V_D, is an exponential curve. The load line (diagonal line) represents the relationship between current and voltage due to Kirchhoff's voltage law applied to the resistor and voltage source, is

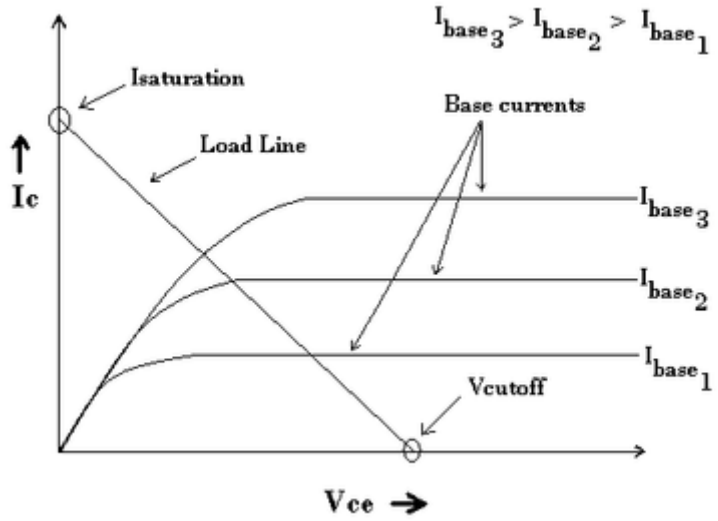
$$V_D = V_{DD} - IR$$

Since the current going through the three elements in series must be the same, and the voltage at the terminals of the diode must be the same, the operating point of the circuit will be at the intersection of the curve with the load line.

In a BJT circuit, the BJT has a different current-voltage (I_C-V_{CE}) characteristic depending on the base current. Placing a series of these curves on the graph shows how the base current will affect the operating point of the circuit.



Transistor load line



Common emitter transistor load line.

The load line diagram at right is for a transistor connected in a common emitter circuit. It shows the collector current in the transistor I_C versus collector voltage V_{CE} for different values of base current I_{base}. The load line represents a particular value of collector load resistor (R_C). The intersections of the load line with the transistor characteristic curve represent the different values of I_C and V_{CE} at different base currents.

The point on the load line where it intersects the collector current axis is referred to as saturation point.[2] At this point, the transistor current is maximum and voltage across collector is minimum, for a given load. For this circuit, $I_{C\text{-}SAT} = V_{CC}/R_C$.[3]

The cutoff point is the point where the load line intersects with the collector voltage axis. Here the transistor current is minimum (approximately zero) and emitter is grounded. Hence $V_{CE\text{-}CUTOFF}=V_{cc}$.

The operating point of the circuit in this configuration is generally designed to be in the active region, approximately between middle of the load line and close to saturation point. In this region, the collector current is proportional to the base current, and hence useful for amplifier applications. a load line is normally drawn on I_c-V_{ce} characteristics curves for the transistor used in amplifier circuit.

Bipolar transistor biasing

Bipolar transistor amplifiers must be properly biased to operate correctly. In circuits made with individual devices (discrete circuits), biasing networks consisting of resistors are commonly employed. Much more elaborate biasing arrangements are used in integrated circuits, for example, bandgap voltage references and current mirrors.

The operating point of a device, also known as bias point, quiescent point, or Q-point, is the point on the output characteristics that shows the DC collector–emitter voltage (V_{ce}) and the collector current (I_c) with no input signal applied. The term is normally used in connection with devices such as transistors.

Bias circuit requirements

Signal requirements for Class A amplifiers

For analog operation of a Class A amplifier, the Q-point is placed so the transistor stays in **active mode** (does not shift to operation in the saturation region or cut-off region) when input is applied. For digital operation, the Q-point is placed so the transistor does the contrary - switches from the "on" (saturation) to the "off" (cutoff) state. Often, the Q-point is established near the center of the active region of a transistor characteristic to allow similar signal swings in positive and negative directions. The Q-point should be stable; in particular, it should be insensitive to variations in transistor parameters (for example, should not shift if transistor is replaced by another of the same type), variations in temperature, variations in power supply voltage and so forth. The circuit must also be practical; both easily implemented and cost-effective.

Thermal considerations

At constant current, the voltage across the emitter–base junction V_{BE} of a bipolar transistor decreases 2 mV (silicon) and 1.8mV

(germanium) for each 1 °C rise in temperature (reference being 25 °C). By the Ebers–Moll model, if the base–emitter voltage V_{BE} is held constant and the temperature rises, the current through the base–emitter diode I_B will increase, and thus the collector current I_C will also increase. Depending on the bias point, the power dissipated in the transistor may also increase, which will further increase its temperature and exacerbate the problem. This deleterious positive feedback results in **thermal runaway**.[1] There are several approaches to mitigate bipolar transistor thermal runaway. For example,

- Negative feedback can be built into the biasing circuit so that increased collector current leads to decreased base current. Hence, the increasing collector current throttles its source.
- Heat sinks can be used that carry away extra heat and prevent the base–emitter temperature from rising.
- The transistor can be biased so that its collector is normally less than half of the power supply voltage, which implies that collector–emitter power dissipation is at its maximum value. Runaway is then impossible because increasing collector current leads to a decrease in dissipated power; this notion is known as the half-voltage principle.

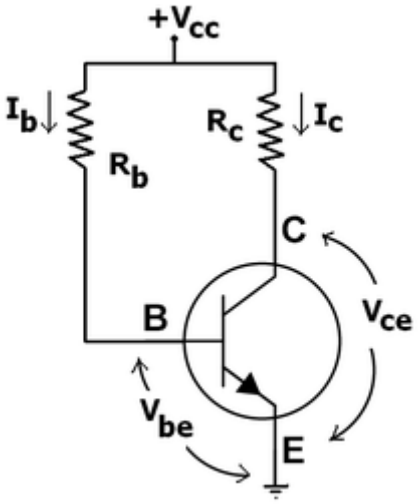
The circuits below primarily demonstrate the use of negative feedback to prevent thermal runaway.

Types of bias circuit for Class A amplifiers

The following discussion treats five common biasing circuits used with Class A bipolar transistor amplifiers:

1. Fixed bias
2. Collector-to-base bias
3. Fixed bias with emitter resistor
4. Voltage divider bias
5. Emitter bias

Fixed bias (base bias)



Fixed bias (Base bias)

This form of biasing is also called base bias. In the example image on the right, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$$V_{cc} = I_B R_B + V_{be}$$

Therefore,

$$I_B = (V_{cc} - V_{be})/R_B$$

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore this type is called fixed bias type of circuit.

Also for given circuit,

$$V_{cc} = I_C R_C + V_{ce}$$

Therefore,

$$V_{ce} = V_{cc} - I_C R_C$$

The common-emitter current gain of a transistor is an important parameter in circuit design, and is specified on the data sheet for a particular transistor. It is denoted as β on this page.

Because

$$I_C = \beta I_B$$

we can obtain I_C as well. In this manner, operating point given as (V_{ce},I_C) can be set for given transistor.

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

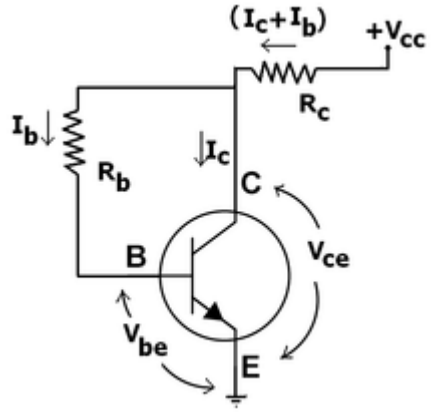
- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.

- Changes in V_{be} will change I_B and thus cause I_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.[citation needed]

Usage:

Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

Collector Feedback Bias



Collector-to-base bias

This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor $R_{\mathrm{B}}$is connected to the collector instead of connecting it to the DC source V_{cc}. So any thermal runaway will induce a voltage drop across the R_{C}resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage $V_{\mathrm{R_b}}$across the base resistor $R_{\mathrm{b}}$is

$$V_{\mathrm{R_b}} = V_{\mathrm{cc}} - \overbrace{(I_{\mathrm{c}} + I_{\mathrm{b}})R_{\mathrm{c}}}^{\text{Voltage drop across } R_{\mathrm{c}}} - \overbrace{V_{\mathrm{be}}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_{\mathrm{c}} = \beta I_{\mathrm{b}}$, and so

$$V_{\mathrm{R_b}} = V_{\mathrm{cc}} - (\overbrace{\beta I_{\mathrm{b}}}^{I_{\mathrm{c}}} + I_{\mathrm{b}})R_{\mathrm{c}} - V_{\mathrm{be}} = V_{\mathrm{cc}} - I_{\mathrm{b}}(\beta + 1)R_{\mathrm{c}} - V_{\mathrm{be}}.$$

From Ohm's law, the base current $I_\mathrm{b} = V_{\mathrm{R_b}}/R_\mathrm{b}$, and so

$$\overbrace{I_\mathrm{b}R_\mathrm{b}}^{V_{\mathrm{R_b}}} = V_\mathrm{cc} - I_\mathrm{b}(\beta+1)R_\mathrm{c} - V_\mathrm{be}.$$

Hence, the base current $I_\mathrm{b}$is

$$I_\mathrm{b} = \frac{V_\mathrm{cc} - V_\mathrm{be}}{R_\mathrm{b} + (\beta+1)R_\mathrm{c}}$$

If $V_\mathrm{be}$is held constant and temperature increases, then the collector current $I_\mathrm{c}$increases. However, a larger $I_\mathrm{c}$causes the voltage drop across resistor $R_\mathrm{c}$to increase, which in turn reduces the voltage $V_{\mathrm{R_b}}$ across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b, which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

- In this circuit, to keep $I_\mathrm{c}$independent of β, the following condition must be met:

$$I_\mathrm{c} = \beta I_\mathrm{b} = \frac{\beta(V_\mathrm{cc} - V_\mathrm{be})}{R_\mathrm{b} + R_\mathrm{c} + \beta R_\mathrm{c}} \approx \frac{(V_\mathrm{cc} - V_\mathrm{be})}{R_\mathrm{c}}$$

which is the case when

$$\beta R_\mathrm{c} \gg R_\mathrm{b}.$$

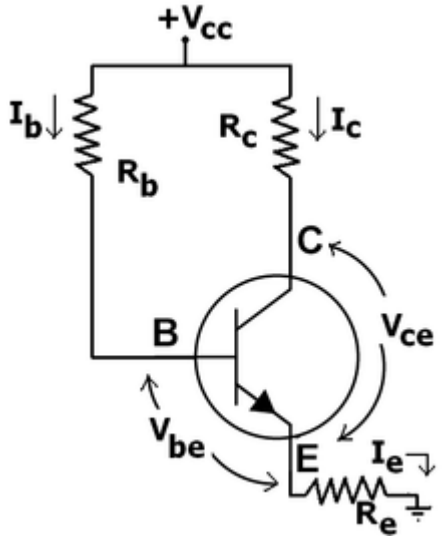
- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making $R_\mathrm{b}$very low.
  - If $R_\mathrm{c}$is large, a high $V_\mathrm{cc}$is necessary, which increases cost as well as precautions necessary while handling.

    - If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.

- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

Fixed bias with emitter resistor



Fixed bias with emitter resistor

The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$$V_{R_b} = V_{CC} - I_e R_e - V_{be}$$

From Ohm's law, the base current is

$$I_b = \frac{V_{R_b}}{R_b}$$

The way feedback controls the bias point is as follows. If V_{be} is held constant and temperature increases, emitter current increases. However, a larger I_e increases the emitter voltage $V_e = I_eR_e$, which in turn reduces the voltage V_{Rb} across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = \beta\ I_B$. Collector current and emitter current are related by $I_c = \alpha\ I_e$ with $\alpha \approx 1$, so the increase in emitter current with temperature is opposed, and the operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in I_C (corresponding to change in β-value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$$I_B = \frac{V_{CC} - V_{be}}{R_B + (\beta + 1)R_E}$$

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if

$$(\beta + 1)R_E \gg R_B$$

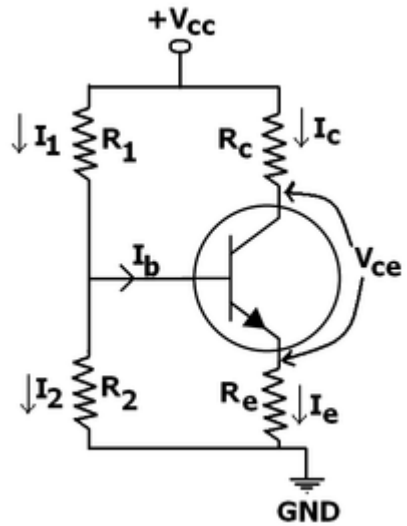
- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.
    - If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
    - If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.
- In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

Usage:

The feedback also increases the input impedance of the amplifier when seen from the base, which can be advantageous. Due to the above disadvantages, this type of biasing circuit is used only with careful consideration of the trade-offs involved.

Collector-Stabilized Biasing

Voltage divider biasing



Voltage divider bias

The voltage divider is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)} \text{provided } I_B << I_2 = V_B/R_2.$$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta\frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if

$$(\beta + 1)R_E >> R_1 \parallel R_2$$

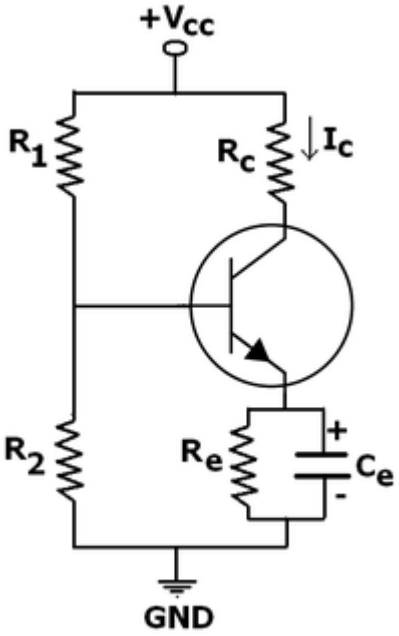
where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \| R_2$ very low.
  - If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
  - If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
- AC as well as DC feedback is caused by R_E, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage:

The circuit's stability and merits as above make it widely used for linear circuits.

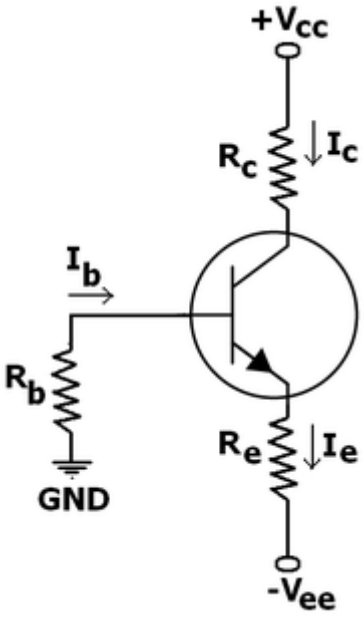
Voltage divider with AC bypass capacitor



Voltage divider with capacitor

The standard voltage divider circuit discussed above faces a drawback - AC feedback caused by resistor R_E reduces the gain. This can be avoided by placing a capacitor (C_E) in parallel with R_E, as shown in circuit diagram.

Emitter bias



Emitter bias

When a split supply (dual power supply) is available, this biasing circuit is the most effective, and provides zero bias voltage at the emitter or collector for load. The negative supply V_{EE} is used to forward-bias the emitter junction through R_E. The positive supply V_{CC} is used to reverse-bias the collector junction. Only two resistors are necessary for the common collector stage and four resistors for the common emitter or common base stage.

We know that,

$V_B - V_E = V_{be}$

If R_B is small enough, base voltage will be approximately zero. Therefore emitter current is,

$I_E = (V_{EE} - V_{be})/R_E$

The operating point is independent of β if $R_E >> R_B/\beta$

Merit:

Good stability of operating point similar to voltage divider bias.

Demerit:

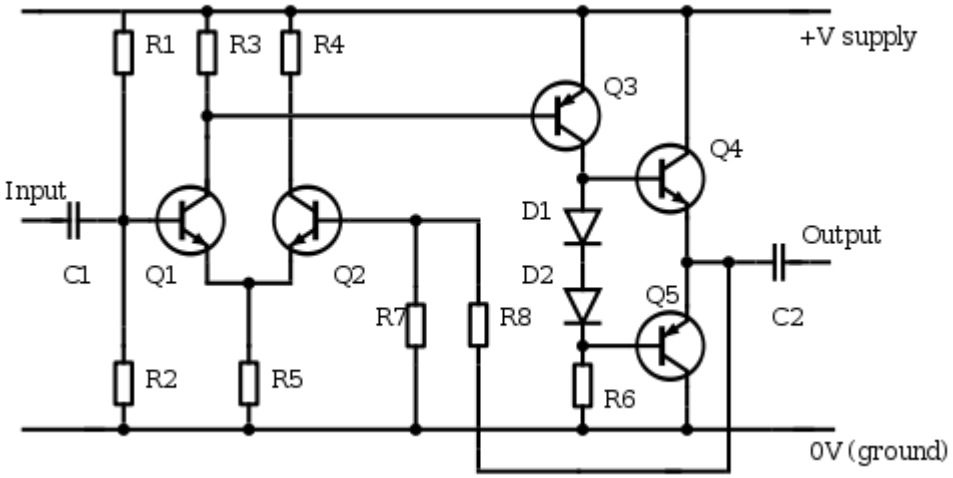
This type can only be used when a split (dual) power supply is available.

Class B and AB amplifiers

Signal requirements

Class B and AB amplifiers employ 2 active devices to cover the complete 360 deg of input signal flow. Each transistor is therefore biased to perform over approximately 180 deg of the input signal. Class B bias is when the collector current I_c with no signal is just conducting (about 1% of maximum possible value). Class AB bias is

when the collector current I_c is about 1/4 of maximum possible value. The class AB push–pull output amplifier circuit below could be the basis for a moderate-power audio amplifier.



A practical amplifier circuit

Q3 is a common emitter stage that provides amplification of the signal and the DC bias current through D1 and D2 to generate a bias voltage for the output devices. The output pair are arranged in Class AB push–pull, also called a complementary pair. The diodes D1 and D2 provide a small amount of constant voltage bias for the output pair, just biasing them into the conducting state so that crossover distortion is minimized. That is, the diodes push the output stage into class-AB mode (assuming that the base-emitter drop of the output transistors is reduced by heat dissipation).

This design automatically stabilizes its operating point, since overall feedback internally operates from DC up through the audio range and beyond. The use of fixed diode bias requires the diodes to be both electrically and thermally matched to the output transistors. If the output transistors conduct too much, they can easily overheat and destroy themselves, as the full current from the power supply is not limited at this stage.

A common solution to help stabilize the output device operating point is to include some emitter resistors, typically an ohm or so. Calculating the values of the circuit's resistors and capacitors is done

based on the components employed and the intended use of the amplifier.

Bias compensation

Temperature Compensation Of BJT Differential AmplifiersThe bipolar junction transistor (BJT) emitter-coupled differential-pair circuit is a familiar amplifier stage in the repertoire of analog designers, but has asurprising obscurity that needs to be revealed. This TechNote examines the emitter-circuit current source, I0, of BJT diff-amps and the effects on amplifier gain of different implementations for it. The widespread belief that a BJT current source can temperature-compensate the diff-amp is true, but the conditions for it do not appearto be widely known, based on most designs

Thermal stability

Thermal stability is the stability of a molecule at high temperatures; i.e. a molecule with more stability has more resistance to decomposition at high temperatures.

Thermal stability also describes, as defined by Schmidt (1928), the stability of a water body and its resistance to mixing. This is the amount of work needed to transform the water body (e.g. a lake) to a uniform water density. The Schmidt stability 'S' is commonly measured in Joule per square meter or g*cm/cm. Compare Stratification.

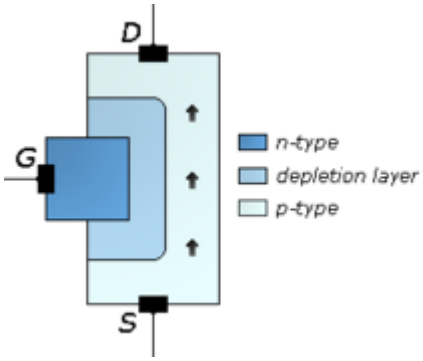
DESIGN FOR BIASING JFET

The **junction gate field-effect transistor** (**JFET** or **JUGFET**) is the simplest type of field-effect transistor. They are three-terminal semiconductor devices that can be used as electronically-controlled switches, amplifiers, or voltage-controlled resistors.

Unlike bipolar transistors, JFETs are exclusively voltage-controlled in that they do not need a biasing current. Electric charge flows through a semiconducting channel between source and drain terminals. By applying a reverse bias voltage to a gate terminal, the channel is "pinched", so that the electric current is impeded or switched off completely. A JFET is usually on when there is no potential difference between its gate and source terminals. If a potential difference of the proper polarity is applied between its gate and source terminals, the JFET will be more resistive to current flow, which means less current would flow in the channel between the source and drain terminals. Thus, JFETs are sometimes referred to as depletion-mode devices.

JFETs can have an n-type or p-type channel. In the n-type, if the voltage applied to the gate is less than that applied to the source, the current will be reduced (similarly in the p-type, if the voltage applied to the gate is greater than that applied to the source). A JFET has a large input impedance (sometimes on the order of 10^{10} ohms), which means that it has a negligible effect on external components or circuits connected to its gate.

Structure

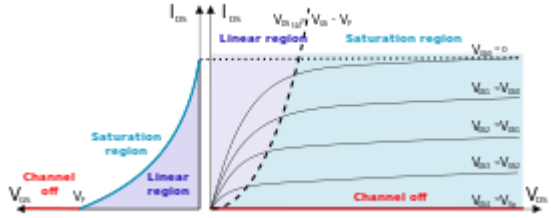


Electric current from source to drain in a **p-channel JFET** is restricted when a voltage is applied to the gate.

The JFET is a long channel of semiconductor material, doped to contain an abundance of positive charge carriers or holes (p-type), or of negative carriers or electrons (n-type). Ohmic contacts at each end

form the source (S) and drain (D). A pn-junction is formed on one or both sides of the channel, or surrounding it, using a region with doping opposite to that of the channel, and biased using an ohmic gate contact (G).

Function



I–V characteristics and output plot of an n-channel JFET

JFET operation is like that of a garden hose. The flow of water through a hose can be controlled by squeezing it to reduce the cross section; the flow of electric charge through a JFET is controlled by constricting the current-carrying channel. The current also depends on the electric field between source and drain (analogous to the difference in pressure on either end of the hose).

Construction of the conducting channel is accomplished using the field effect: a voltage between the gate and source is applied to reverse bias the gate-source pn-junction, thereby widening the depletion layer of this junction (see top figure), encroaching upon the conducting channel and restricting its cross-sectional area. The depletion layer is so-called because it is depleted of mobile carriers and so is electrically non-conducting for practical purposes.[1]

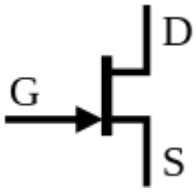
When the depletion layer spans the width of the conduction channel, "pinch-off" is achieved and drain to source conduction stops. Pinch-off occurs at a particular reverse bias (V_{GS}) of the gate-source junction. The pinch-off voltage (V_p) varies considerably, even among devices of the same type. For example, $V_{GS(off)}$ for the Temic J202 device varies from −0.8 V to −4 V.[2] Typical values vary from −0.3 V to −10 V.

To switch off an **n**-channel device requires a **n**egative gate-source voltage (V_{GS}). Conversely, to switch off a **p**-channel device requires **p**ositive V_{GS}.

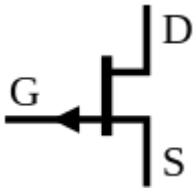
In normal operation, the electric field developed by the gate blocks source-drain conduction to some extent.

Some JFET devices are symmetrical with respect to the source and drain.

Schematic symbols



Circuit symbol for an n-Channel JFET



Circuit symbol for a p-Channel JFET

The JFET gate is sometimes drawn in the middle of the channel (instead of at the drain or source electrode as in these examples). This symmetry suggests that "drain" and "source" are interchangeable, so the symbol should be used only for those JFETs where they are indeed interchangeable.

Officially, the style of the symbol should show the component inside a circle (representing the envelope of a discrete device). This is true in both the US and Europe. The symbol is usually drawn without the circle when drawing schematics of integrated circuits. More recently, the symbol is often drawn without its circle even for discrete devices.

In every case the arrow head shows the polarity of the P-N junction formed between the channel and gate. As with an ordinary diode, the arrow points from P to N, the direction of conventional current when forward-biased. An English mnemonic is that the arrow of an N-channel device "points i**n**".

Comparison with other transistors

At room temperature, JFET gate current (the reverse leakage of the gate-to-channel junction) is comparable to that of a MOSFET (which has insulating oxide between gate and channel), but much less than the base current of a bipolar junction transistor. The JFET has higher transconductance than the MOSFET, as well as lower flicker noise, and is therefore used in some low-noise, high input-impedance op-amps.

History of the JFET

The JFET was predicted by Julius Lilienfeld in 1925 and by the mid-1930s its theory of operation was sufficiently well known to justify a patent. However, it was not possible for many years to make doped crystals with enough precision to show the effect. In 1947, researchers John Bardeen, Walter Houser Brattain, and William Shockley were trying to make a JFET when they discovered the point-contact transistor. The first practical JFETs were made many years later, in spite of their conception long before the junction transistor. To some extent it can be treated as a hybrid of a MOSFET (metal–oxide–semiconductor field-effect transistor) and a BJT though an IGBT resembles more of the hybrid features.

Mathematical model

The current in N-JFET due to a small voltage V_{DS} (that is, in the linear ohmic region) is given by treating the channel as a rectangular bar of material of electrical conductivity $qN_d\mu_n$:[3]

$$I_D = \frac{bW}{L} qN_d\mu_n V_{DS}$$

where

I_D = drain–source current

b = channel thickness for a given gate voltage

W = channel width

L = channel length

q = electron charge = 1.6 x 10^{-19} C

μ_n = electron mobility

N_d = n-type doping (donor) concentration

The drain current in the saturation region is often approximated in terms of gate bias as:[3]

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where

I_{DSS} is the saturation current at zero gate–source voltage.[clarification needed]

In the saturation region, the JFET drain current is most significantly affected by the gate–source voltage and barely affected by the drain–source voltage.

If the channel doping is uniform, such that the depletion region thickness will grow in proportion to the square root of (the absolute value of) the gate–source voltage, then the channel thickness b can be expressed in terms of the zero-bias channel thickness a as:[citation needed]

$$b = a\left(1 - \sqrt{\frac{V_{GS}}{V_P}}\right)$$

where

V_P is the pinchoff voltage, the gate–source voltage at which the channel thickness goes to zero

a is the channel thickness at zero gate–source voltage.

Then the drain current in the linear ohmic region can be expressed as:

$$I_D = \frac{bW}{L} q N_d \mu_n V_{DS} = \frac{aW}{L} q N_d \mu_n \left(1 - \sqrt{\frac{V_{GS}}{V_P}}\right) V_{DS}$$

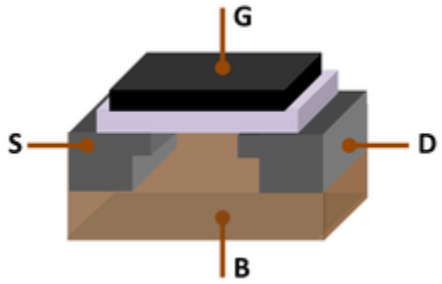
or (in terms of I_{DSS}):[citation needed]

$$I_D = \frac{2 I_{DSS}}{V_P^2} \left(V_{GS} - V_P - \frac{V_{DS}}{2}\right) V_{DS}$$

DESIGN OF BIASING MOSFET

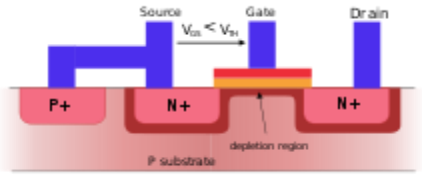
MOSFET

From Wikipedia, the free encyclopedia

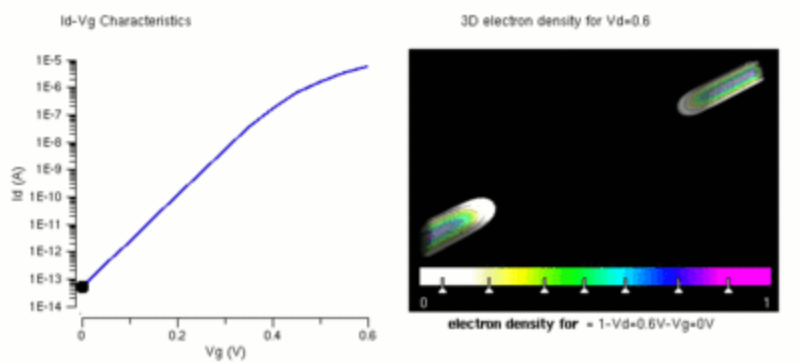


MOSFET showing gate (G), body (B), source (S) and drain (D) terminals. The gate is separated from the body by an insulating layer (white)

Two power MOSFETs in the surface-mount package D2PAK. Operating as switches, each of these components can sustain a blocking voltage of 120 volts in the OFF state, and can conduct a continuous current of 30 amperes in the ON state, dissipating up up to about 100 watts and controlling a load of over 2000 watts. A matchstick is pictured for scale.



A cross section through an nMOSFET when the gate voltage V_{GS} is below the threshold for making a conductive channel; there is little or no conduction between the terminals drain and source; the switch is off. When the gate is more positive, it attracts electrons, inducing an n-type conductive channel in the substrate below the oxide, which allows electrons to flow between the n-doped terminals; the switch is on.



Simulation result for formation of inversion channel (electron density) and attainment of threshold voltage (IV) in a nanowire MOSFET. Note that the threshold voltage for this device lies around 0.45 V.

The **metal–oxide–semiconductor field-effect transistor** (**MOSFET**, **MOS-FET**, or **MOS FET**) is a type of transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals,[1] the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common.

In enhancement mode MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts via the field effect. The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the inversion layer. The channel can contain electrons (called an nMOSFET or nMOS), or holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate (see article on semiconductor devices). In the less common depletion mode MOSFET, detailed later on, the channel consists of carriers in a surface impurity layer of opposite type to the substrate, and

conductivity is decreased by application of a field that depletes carriers from this surface layer.[2]

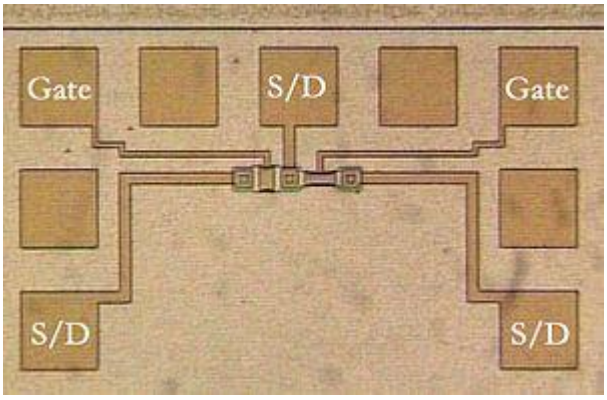
The "metal" in the name MOSFET is now often a misnomer because the previously metal gate material is now often a layer of polysilicon (polycrystalline silicon). Aluminium had been the gate material until the mid-1970s, when polysilicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity, since it is difficult to increase the speed of operation of transistors without metal gates.

Likewise, the "oxide" in the name can be a misnomer, as different dielectric materials are used with the aim of obtaining strong channels with smaller applied voltages.

An insulated-gate field-effect transistor or **IGFET** is a related term almost synonymous with MOSFET. The term may be more inclusive, since many "MOSFETs" use a gate that is not metal, and a gate insulator that is not oxide. Another synonym is MISFET for metal–insulator–semiconductor FET.

The basic principle of the field-effect transistor was first patented by Julius Edgar Lilienfeld in 1925.

Composition



Photomicrograph of two metal-gate MOSFETs in a test pattern. Probe pads for two gates and three source/drain nodes are labeled.

Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM and Intel, recently started using a chemical compound of silicon and germanium (SiGe) in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces, thus are not suitable for MOSFETs. Research continues on creating insulators with acceptable electrical characteristics on other semiconductor material.

In order to overcome the increase in power consumption due to gate current leakage, a high-κ dielectric is used instead of silicon dioxide for the gate insulator, while polysilicon is replaced by metal gates (see Intel announcement[3]).

The gate is separated from the channel by a thin insulating layer, traditionally of silicon dioxide and later of silicon oxynitride. Some companies have started to introduce a high-κ dielectric + metal gate combination in the 45 nanometer node.

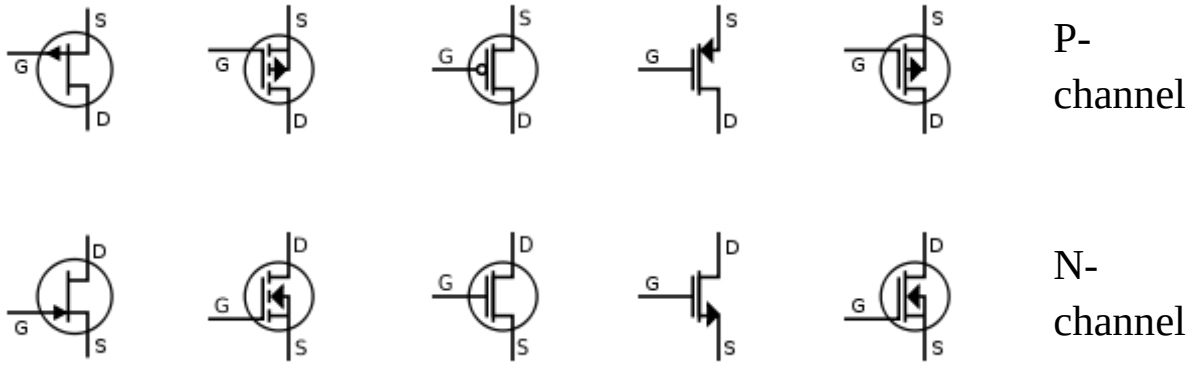
When a voltage is applied between the gate and body terminals, the electric field generated penetrates through the oxide and creates an "inversion layer" or "channel" at the semiconductor-insulator interface. The inversion channel is of the same type, p-type or n-type, as the source and drain, thus it provides a channel through which current can pass. Varying the voltage between the gate and body modulates the conductivity of this layer and thereby controls the current flow between drain and source.

Circuit symbols

A variety of symbols are used for the MOSFET. The basic design is generally a line for the channel with the source and drain leaving it at right angles and then bending back at right angles into the same direction as the channel. Sometimes three line segments are used for enhancement mode and a solid line for depletion mode. (see Depletion and enhancement modes) Another line is drawn parallel to the channel for the gate.

The "bulk" or "body" connection, if shown, is shown connected to the back of the channel with an arrow indicating PMOS or NMOS. Arrows always point from P to N, so an NMOS (N-channel in P-well or P-substrate) has the arrow pointing in (from the bulk to the channel). If the bulk is connected to the source (as is generally the case with discrete devices) it is sometimes angled to meet up with the source leaving the transistor. If the bulk is not shown (as is often the case in IC design as they are generally common bulk) an inversion symbol is sometimes used to indicate PMOS, alternatively an arrow on the source may be used in the same way as for bipolar transistors (out for nMOS, in for pMOS).

Comparison of enhancement-mode and depletion-mode MOSFET symbols, along with JFET symbols. The orientation of the symbols, (most significantly the position of source relative to drain) is such that more positive voltages appear higher on the page than less positive voltages, implying current flowing "down" the page:[4][5][6]



JFET | MOSFET enh | MOSFET enh (no bulk) | MOSFET dep

In schematics where G, S, D are not labeled, the detailed features of the symbol indicate which terminal is source and which is drain. For enhancement-mode and depletion-mode MOSFET symbols (in columns two and five), the source terminal is the one connected to the triangle. Additionally, in this diagram, the gate is shown as an "L" shape, whose input leg is closer to S than D, also indicating which is

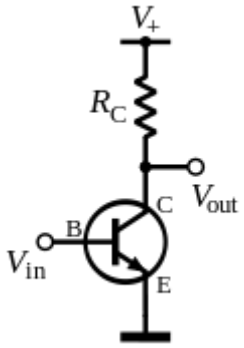
which. However, these symbols are often drawn with a "T" shaped gate (as elsewhere on this page), so it is the triangle which must be relied upon to indicate the source terminal.

For the symbols in which the bulk, or body, terminal is shown, it is here shown internally connected to the source (i.e., the black triangles in the diagrams in columns 2 and 5). This is a typical configuration, but by no means the only important configuration. In general, the MOSFET is a four-terminal device, and in integrated circuits many of the MOSFETs share a body connection, not necessarily connected to the source terminals of all the transistors.

UNIT-2 BJT AMPLIFIERS

In electronics, a **common emitter** amplifier is one of three basic single-stage bipolar-junction-transistor (BJT) amplifier topologies, typically used as a voltage amplifier.

In this circuit the base terminal of the transistor serves as the input, the collector is the output, and the emitter is common to both (for example, it may be tied to ground reference or a power supply rail), hence its name. The analogous field-effect transistor circuit is the common source amplifier, and the analogous tube circuit is the common cathode amplifier.



Emitter degeneration

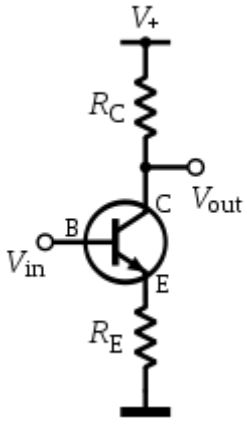


Figure 2: Adding an emitter resistor decreases gain, but increases linearity and stability

Common emitter amplifiers give the amplifier an inverted output and can have a very high gain that may vary widely from one transistor to the next. The gain is a strong function of both temperature and bias current, and so the actual gain is somewhat unpredictable. Stability is another problem associated with such high gain circuits due to any unintentional positive feedback that may be present.

Other problems associated with the circuit are the low input dynamic range imposed by the small-signal limit; there is high distortion if this limit is exceeded and the transistor ceases to behave like its small-signal model. One common way of alleviating these issues is with the use of negative feedback, which is usually implemented with emitter degeneration. Emitter degeneration refers to the addition of a small resistor (or any impedance) between the emitter and the common signal source (e.g., the ground reference or a power supply rail). This impedance $R_\mathrm{E}$reduces the overall transconductance $G_m = g_m$of the circuit by a factor of $g_m R_\mathrm{E} + 1$, which makes the voltage gain

$$A_\mathrm{v} \triangleq \frac{v_\mathrm{out}}{v_\mathrm{in}} = \frac{-g_m R_\mathrm{C}}{g_m R_\mathrm{E} + 1} \approx -\frac{R_\mathrm{C}}{R_\mathrm{E}} \qquad (\text{where} \quad g_m R_\mathrm{E} \gg 1).$$

So the voltage gain depends almost exclusively on the ratio of the resistors $R_\mathrm{C}/R_\mathrm{E}$rather than the transistor's intrinsic and unpredictable characteristics. The distortion and stability characteristics of the circuit are thus improved at the expense of a reduction in gain.

Characteristics

At low frequencies and using a simplified hybrid-pi model, the following small-signal characteristics can be derived.

Definition	Expression (with emitter degeneration)	Expression (without emitter degeneration, i.e.,

			$R_E = 0$)
Current gain	$A_\mathrm{i} \triangleq \frac{i_\mathrm{out}}{i_\mathrm{in}}$	β	β
Voltage gain	$A_\mathrm{v} \triangleq \frac{v_\mathrm{out}}{v_\mathrm{in}}$	$-\frac{\beta R_\mathrm{C}}{r_\pi + (\beta+1)R_\mathrm{E}}$	$\approx -g_m R_\mathrm{C}$
Input impedance	$r_\mathrm{in} \triangleq \frac{v_\mathrm{in}}{i_\mathrm{in}}$	$r_\pi + (\beta+1)R_\mathrm{E}$	r_π
Output impedance	$r_\mathrm{out} \triangleq \frac{v_\mathrm{out}}{i_\mathrm{out}}$	R_C	R_C

If the emitter degeneration resistor is not present, then $R_\mathrm{E} = 0\,\Omega$, and the expressions effectively simplify to the ones given by the rightmost column (note that the voltage gain is an ideal value; the actual gain is somewhat unpredictable). As expected, when $R_\mathrm{E}$is increased, the input impedance is increased and the voltage gain $A_\mathrm{v}$is reduced.

Bandwidth

The bandwidth of the common-emitter amplifier tends to be low due to high capacitance resulting from the Miller effect. The parasitic base-collector capacitance $C_\mathrm{CB}$appears like a larger parasitic capacitor $C_\mathrm{CB}(1 - A_\mathrm{v})$(where $A_\mathrm{v}$is negative) from the base to ground.[1] This large capacitor greatly decreases the bandwidth of the amplifier as it makes the time constant of the parasitic input RC filter $r_\mathrm{s}(1 - A_\mathrm{V})C_\mathrm{CB}$where $r_\mathrm{s}$is the output impedance of the signal source connected to the ideal base.

The problem can be mitigated in several ways, including:

- Reduction of the voltage gain magnitude $|A_\mathrm{v}|$ (e.g., by using emitter degeneration).

- Reduction of the output impedance r_s of the signal source connected to the base (e.g., by using an emitter follower or some other voltage follower).
- Using a cascode configuration, which inserts a low input impedance current buffer (e.g. a common base amplifier) between the transistor's collector and the load. This configuration holds the transistor's collector voltage roughly constant, thus making the base to collector gain zero and hence (ideally) removing the Miller effect.
- Using a differential amplifier topology like an emitter follower driving a grounded-base amplifier; as long as the emitter follower is truly a common-collector amplifier, the Miller effect is removed.

The Miller effect negatively affects the performance of the common source amplifier in the same way (and has similar solutions).When an AC signal is applied to the transistor amplifier it causes the base voltage VB to fluctuate in value at the AC signal. The positive half of the applied signal will cause an increase in the value of VB this turn will increase the base current IB and cause a corresponding increase in emitter current IE and collector current IC. As a result, the collector emitter voltage will be reduced because of the increase voltage drop across RL. The negative alternation of an AC signal will cause a decrease in IB this action then causes a corresponding decrease in IE through RL. The output signal of a common- emitter amplifier is therefore 180 degrees out of phase with the input signal.

It is also named common- emitter amplifier because the emitter of the transistor is common to both the input circuit and output circuit. The input signal is applied across the ground and the base circuit of the transistor. The output signal appears across ground and the collector of the transistor. Since the emitter is connected to the ground, it is common to signals, input and output.

The common- emitter circuit is the most widely used of junction, transistor amplifiers. As compared with the common- base connection, it has higher input impedance and lower output impedance. A single power supply is easily used for biasing. In

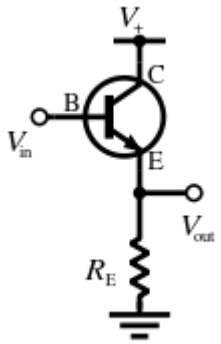
addition, higher voltage and power gains are usually obtained for common- emitter (CE) operation.

Current gain in the common emitter circuit is obtained from the base and the collector circuit currents. Because a very small change in base current produces a large change in collector current, the current gain (β) is always greater than unity for the common-emitter circuit, a typical value is about 50.

SMALL SIGNAL ANALYSIS OF CC AMP

In electronics, a **common collector** amplifier (also known as an **emitter follower**) is one of three basic single-stage bipolar junction transistor (BJT) amplifier topologies, typically used as a voltage buffer.

In this circuit the base terminal of the transistor serves as the input, the emitter is the output, and the collector is common to both (for example, it may be tied to ground reference or a power supply rail), hence its name. The analogous field-effect transistor circuit is the common drain amplifier



Basic circuit

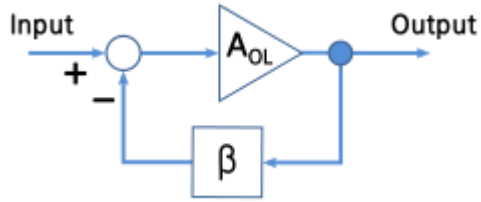


Figure 2: A negative feedback amplifier

The circuit can be explained by viewing the transistor as being under the control of negative feedback. From this viewpoint, a common collector stage (Fig. 1) is an amplifier with full series negative feedback. In this configuration (Fig. 2 with $\beta = 1$), the entire output voltage V_{OUT} is placed contrary and in series with the input voltage V_{IN}. Thus the two voltages are subtracted according to KVL (the subtractor from the function block diagram is implemented just by the input loop) and their difference Vdiff = V_{IN} - V_{OUT} is applied to the base-emitter junction. The transistor monitors continuously Vdiff and adjusts its emitter voltage almost equal (less V_{BEO}) to the input voltage by passing the according collector current through the emitter resistor R_E. As a result, the output voltage follows the input voltage variations from V_{BEO} up to V_+; hence the name, emitter follower.

Intuitively, this behavior can be also understood by realizing that the base-emitter voltage in the bipolar transistor is very insensitive to bias changes, so any change in base voltage is transmitted (to good approximation) directly to the emitter. It depends slightly on various disturbances (transistor tolerances, temperature variations, load resistance, collector resistor if it is added, etc.) since the transistor reacts to these disturbances and restores the equilibrium. It never saturates even if the input voltage reaches the positive rail.

The common collector circuit can be shown mathematically to have a voltage gain of almost unity:

$$A_v = \frac{v_{out}}{v_{in}} \approx 1$$

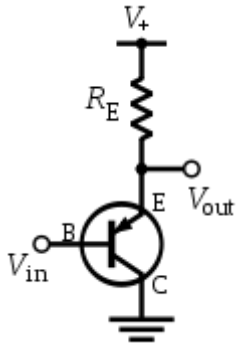


Figure 3: PNP version of the emitter follower circuit, all polarities are reversed.

A small voltage change on the input terminal will be replicated at the output (depending slightly on the transistor's gain and the value of the load resistance; see gain formula below). This circuit is useful because it has a large input impedance, so it will not load down the previous circuit:

$$r_{\mathrm{in}} \approx \beta_0 R_{\mathrm{E}}$$

and a small output impedance, so it can drive low-resistance loads:

$$r_{\mathrm{out}} \approx R_{\mathrm{E}} \| \frac{R_{\mathrm{source}}}{\beta_0}$$

Typically, the emitter resistor is significantly larger and can be removed from the equation:

$$r_{\mathrm{out}} \approx \frac{R_{\mathrm{source}}}{\beta_0}$$

Applications

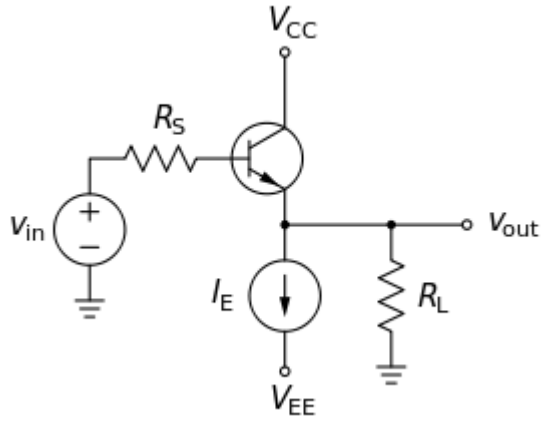


Figure 4: NPN voltage follower with current source biasing suitable for integrated circuits

The low output impedance allows a source with a large output impedance to drive a small load impedance; it functions as a voltage buffer. In other words, the circuit has current gain (which depends largely on the h_{FE} of the transistor) instead of voltage gain. A small change to the input current results in much larger change in the output current supplied to the output load.

One aspect of buffer action is transformation of impedances. For example, the Thévenin resistance of a combination of a voltage follower driven by a voltage source with high Thévenin resistance is reduced to only the output resistance of the voltage follower (a small resistance). That resistance reduction makes the combination a more ideal voltage source. Conversely, a voltage follower inserted between a small load resistance and a driving stage presents a large load to the driving stage—an advantage in coupling a voltage signal to a small load.

This configuration is commonly used in the output stages of class-B and class-AB amplifiers. The base circuit is modified to operate the transistor in class-B or AB mode. In class-A mode, sometimes an active current source is used instead of R_E (Fig. 4) to improve linearity and/or efficiency.[1]

Characteristics

At low frequencies and using a simplified hybrid-pi model, the following small-signal characteristics can be derived. (Parameter $\beta = g_m r_\pi$ and the parallel lines indicate components in parallel.)

	Definition	Expression	Approximate expression	Conditions
Current gain	$A_\mathrm{i} = \frac{i_\mathrm{out}}{i_\mathrm{in}}$	$\beta_0 + 1$	$\approx \beta_0$	$\beta_0 \gg 1$
Voltage	$A_\mathrm{v} = \frac{v_\mathrm{out}}{v_\mathrm{in}}$	$\frac{g_m R_\mathrm{E}}{g_m R_\mathrm{E} + 1}$	≈ 1	$g_m R_\mathrm{E} \gg 1$

gain

Input resistance $r_{\text{in}} = \frac{v_{\text{in}}}{i_{\text{in}}} \; r_\pi + (\beta_0 + 1) R_{\text{E}} \; \approx \beta_0 R_{\text{E}} \qquad (g_m R_{\text{E}} \gg 1) \wedge (\beta_0 \gg$

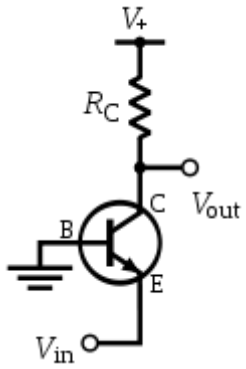
Output resistance $r_{\text{out}} = \frac{v_{\text{ou}}}{i_{\text{ou}}} R_{\text{E}} \parallel \left(\frac{r_\pi + R_{\text{sou}}}{\beta_0 + 1} \approx \frac{1}{g_m} + \frac{R_{\text{sou}}}{\beta_0} (\beta_0 \gg 1) \wedge (r_{\text{in}} \gg R_{\text{sc}}$

Where R_{source} is the Thévenin equivalent source resistance.

SMALL SIGNAL ANALYSIS OF CB AMP

In electronics, a **common base** (also known as **grounded-base**) amplifier is one of three basic single-stage bipolar junction transistor (BJT) amplifier topologies, typically used as a current buffer or voltage amplifier.

In this circuit the emitter terminal of the transistor serves as the input, the collector the output, and the base is connected to ground, or "common", hence its name. The analogous field-effect transistor circuit is the common gate amplifier



Simplified Operation

As current is sunk from the emitter this provides potential difference so causing the transistor to conduct.[1] The current conducted via the collector is proportional to the voltage across the base-emitter junction, accounting for the bias, as with other configurations.[2]

Therefore, if no current is sunk at the emitter the transistor does not conduct.

Applications

This arrangement is not very common in low-frequency circuits, where it is usually employed for amplifiers that require an unusually low input impedance, for example to act as a preamplifier for moving-coil microphones. However, it is popular in high-frequency amplifiers, for example for VHF and UHF, because its input capacitance does not suffer from the Miller effect, which degrades the bandwidth of the common emitter configuration, and because of the relatively high isolation between the input and output. This high isolation means that there is little feedback from the output back to the input, leading to high stability.

This configuration is also useful as a current buffer since it has a current gain of approximately unity (see formulas below). Often a common base is used in this manner, preceded by a common emitter stage. The combination of these two form the cascode configuration, which possesses several of the benefits of each configuration, such as high input impedance and isolation.

Low-frequency characteristics

At low frequencies and under small-signal conditions, the circuit in Figure 1 can be represented by that in Figure 2, where the hybrid-pi model for the BJT has been employed. The input signal is represented by a Thévenin voltage source, v_s, with a series resistance R_s and the load is a resistor R_L. This circuit can be used to derive the following characteristics of the common base amplifier.

	Definition	Expression	Approximate expression	Conditions
Open-circuit voltage gain		$A_v = \frac{v_o}{v_i}\Big\vert_{R} \frac{(g_m r_O+1)R_C}{R_C+r_O}$	$g_m R_C$	$r_O \gg R_C$
Short-circuit current gain		$A_i = \frac{i_o}{i_i}\Big\vert_{R} \frac{r_\pi+\beta r_O}{r_\pi+(\beta+1)r_O}$	1	$\beta \gg 1$
Input resistance		$R_{\text{in}} = \frac{v_i}{i_i} \quad \frac{(r_O+R_C\|R_L)r_E}{r_O+r_E+\frac{R_C\|R_L}{\beta+1}}$	$r_E \left(\approx \frac{1}{g_m}\right)$	$r_O \gg R_C\|R_L$
Output resistance		$R_{\text{out}} = \frac{v_o}{-i} R_C\|\{[1+g_m(r_\pi\|R_S)]r$	$R_C\|\|r_O$	$R_S \ll r_E$
			$R_C\|\|[(r_\pi\|\|R_S)(1$	$R_S \gg r_E$

Note: Parallel lines (||) indicate components in parallel.

In general the overall voltage/current gain may be substantially less than the open/short circuit gains listed above (depending on the source and load resistances) due to the loading effect.

Active loads

For voltage amplification, the range of allowed output voltage swing in this amplifier is tied to its voltage gain when a resistor load R_C is employed, as in Figure 1. That is, large voltage gain requires large R_C, and that in turn implies a large DC voltage drop across R_C. For a given supply voltage, the larger this drop, the smaller the transistor V_{CB} and the less output swing is allowed before saturation of the transistor occurs, with resultant distortion of the output signal. To avoid this situation, an active load can be used, for example, a current mirror. If this choice is made, the value of R_C in the table above is replaced by the small-signal output resistance of the active load, which is generally at least as large as the r_O of the active transistor in Figure 1. On the other hand, the DC voltage drop across the active load is a fixed low value (the **compliance voltage** of the active load), much less than the DC voltage drop incurred for comparable gain using a resistor R_C. That is, an active load imposes less restriction on the output voltage swing. Notice that active load or not, large AC gain still is coupled to large AC output resistance, which leads to poor voltage division at the output except for large loads $R_L >> R_{out}$.

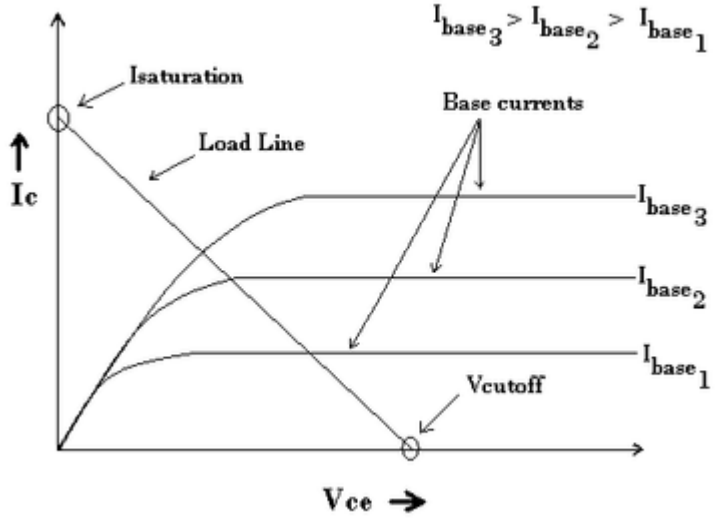
For use as a current buffer, gain is not affected by R_C, but output resistance is. Because of the current division at the output, it is desirable to have an output resistance for the buffer much larger than the load R_L being driven so large signal currents can be delivered to a load. If a resistor R_C is used, as in Figure 1, a large output resistance is coupled to a large R_C, again limiting the signal swing at the output. (Even though current is delivered to the load, usually a large current signal into the load implies a large voltage swing across the load as well.) An active load provides high AC output resistance with much less serious impact upon the amplitude of output signal swing.

AC LOADLINE

Semiconductor circuits typically have both DC and AC currents in them, with a source of DC current to bias the nonlinear semiconductor to the correct operating point, and the AC signal superimposed on the DC. Load lines can be used separately for both DC and AC analysis. The DC load line is the load line of the DC equivalent circuit, defined by reducing the reactive components to zero (replacing capacitors by

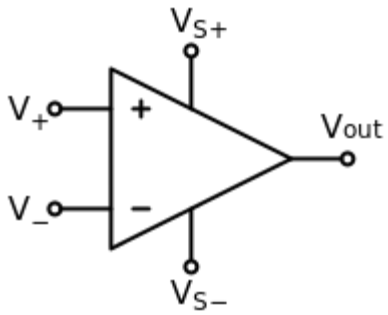
open circuits and inductors by closed circuits). It is used to determine the correct DC operating point, often called the Q point.

Once a DC operating point is defined by the DC load line, an AC load line can be drawn through the Q point. The AC load line is a straight line with a slope equal to the AC impedance facing the nonlinear device, which is in general different from the DC resistance. The ratio of AC voltage to current in the device is defined by this line. Because the impedance of the reactive components will vary with frequency, the slope of the AC load line depends on the frequency of the applied signal. So there are many AC load lines, that vary from the DC load line (at low frequency) to a limiting AC load line, all having a common intersection at the dc operating point. This limiting load line, generally referred to as the AC load line, is the load line of the circuit at "infinite frequency", and can be found by replacing capacitors with short circuits, and inductors with open circuits.



DIFFERENTIAL AMP

A **differential amplifier** is a type of electronic amplifier that amplifies the difference between two voltages but does not amplify the particular voltages.



Theory

Many electronic devices use differential amplifiers internally. The output of an ideal differential amplifier is given by:

$$V_{\text{out}} = A_{\text{d}}(V_{\text{in}}^{+} - V_{\text{in}}^{-})$$

Where V_{in}^{+} and V_{in}^{-} are the input voltages and A_{d} is the differential gain. In practice, however, the gain is not quite equal for the two inputs. This means, for instance, that if V_{in}^{+} and V_{in}^{-} are equal, the output will not be zero, as it would be in the ideal case. A more realistic expression for the output of a differential amplifier thus includes a second term.

$$V_{\text{out}} = A_{\text{d}}(V_{\text{in}}^{+} - V_{\text{in}}^{-}) + A_{\text{c}}\left(\frac{V_{\text{in}}^{+} + V_{\text{in}}^{-}}{2}\right)$$

A_{c} is called the common-mode gain of the amplifier. As differential amplifiers are often used to null out noise or bias-voltages that appear at both inputs, a low common-mode gain is usually desired.

The common-mode rejection ratio (CMRR), usually defined as the ratio between differential-mode gain and common-mode gain, indicates the ability of the amplifier to accurately cancel voltages that are common to both inputs. The common-mode rejection ratio is defined as:

$$\text{CMRR} = 10\log_{10}\left(\frac{A_{\text{d}}}{A_{\text{c}}}\right)^{2} = 20\log_{10}\left(\frac{A_{\text{d}}}{|A_{\text{c}}|}\right)$$

In a perfectly symmetrical differential amplifier, A_c is zero and the CMRR is infinite. Note that a differential amplifier is a more general form of amplifier than one with a single input; by grounding one input of a differential amplifier, a single-ended amplifier results.

Long-tailed pair

Historical background

Differential amplifiers are usually implemented with a basic circuit called long-tailed pair. This circuit was originally implemented using a pair of vacuum tubes. The circuit works the same way for all three-terminal devices with current gain. The long-tail resistor circuit bias points are largely determined by Ohm's Law and less so by active component characteristics.

The long-tailed pair was developed from earlier knowledge of push-pull circuit techniques and measurement bridges.[1] An early circuit which closely resembles a long-tailed pair was published by Matthews in 1934,[2] and it seems likely that this was intended to be a true long-tailed pair but was published with a drawing error. The earliest definite long-tailed pair circuit appears in a patent submitted by Alan Blumlein in 1936.[3] By the end of the 1930s the topology was well established and had been described by various authors including Offner (1937),[4] Schmitt (1937)[5] and Toennies (1938) and it was particularly used for detection and measurement of physiological impulses.[6]

The long-tailed pair was very successfully used in early British computing, most notably the Pilot ACE model and descendants,[nb 1] Wilkes' EDSAC, and probably others designed by people who worked with Blumlein or his peers. The long-tailed pair has many attributes as a switch: largely immune to tube (transistor) variations (of great importance when machines contained 1,000 or more tubes), high gain, gain stability, high input impedance, medium/low output impedance, good clipper (with not-too-long tail), non-inverting (EDSAC contained no inverters!) and large output voltage swings. One disadvantage is that the output voltage swing (typically ±10–20 V)

was imposed upon a high DC voltage (200 V or so), requiring care in signal coupling, usually some form of wide-band DC coupling. Many computers of this time tried to avoid this problem by using only AC-coupled pulse logic, which made them very large and overly complex (ENIAC: 18,000 tubes for a 20 digit calculator) or unreliable. DC-coupled circuitry became the norm after the first generation of vacuum tube computers.

Configurations

A differential (long-tailed,[nb 2] emitter-coupled) pair amplifier consists of two amplifying stages with common (emitter, source or cathode) degeneration.

Differential output

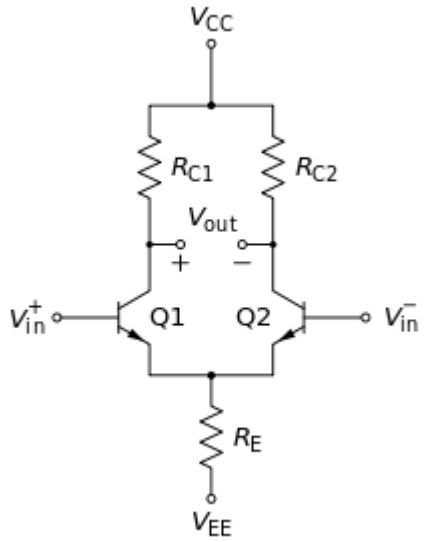


Figure 2: A classic long-tailed pair

With two inputs and two outputs, this forms a differential amplifier stage (Fig. 2). The two bases (or grids or gates) are inputs which are differentially amplified (subtracted and multiplied) by the pair; they can be fed with a differential (balanced) input signal, or one input could be grounded to form a phase splitter circuit. An amplifier with differential output can drive floating load or another stage with differential input.

Single-ended output

If the differential output is not desired, then only one output can be used (taken from just one of the collectors (or anodes or drains), disregarding the other output without a collector inductor; this configuration is referred to as single-ended output. The gain is half that of the stage with differential output. To avoid sacrificing gain, a differential to single-ended converter can be utilized. This is often implemented as a current mirror (Fig. 3).

Operation

To explain the circuit operation, four particular modes are isolated below although, in practice, some of them act simultaneously and their effects are superimposed.

Biasing

In contrast with classic amplifying stages that are biased from the side of the base (and so they are highly β-dependent), the differential pair is directly biased from the side of the emitters by sinking/injecting the total quiescent current. The series negative feedback (the emitter degeneration) makes the transistors act as voltage stabilizers; it forces them to adjust their V_{BE} voltages (base currents) to pass the quiescent current through their collector-emitter junctions.[nb 3] So, due to the negative feedback, the quiescent current depends slightly on the transistor's β.

The biasing base currents needed to evoke the quiescent collector currents usually come from the ground, pass through the input sources and enter the bases. So, the sources have to be galvanic (DC) to ensure paths for the biasing currents and low resistive enough to not create significant voltage drops across them. Otherwise, additional DC elements should be connected between the bases and the ground (or the positive power supply).

Common mode

At common mode (the two input voltages change in the same directions), the two voltage (emitter) followers cooperate with each other working together on the common high-resistive emitter load (the "long tail"). They all together increase or decrease the voltage of the common emitter point (figuratively speaking, they together "pull up" or "pull down" it so that it moves). In addition, the dynamic load "helps" them by changing its instant ohmic resistance in the same direction as the input voltages (it increases when the voltage increases and vice versa.) thus keeping up constant total resistance between the two supply rails. There is a full (100%) negative feedback; the two input base voltages and the emitter voltage change simultaneously while the collector currents and the total current do not change. As a result, the output collector voltages do not change as well.

Differential mode

Normal. At differential mode (the two input voltages change in opposite directions), the two voltage (emitter) followers oppose each other - while one of them tries to increase the voltage of the common emitter point, the other tries to decrease it (figuratively speaking, one of them "pulls up" the common point while the other "pulls down" it so that it stays immovable) and v.v. So, the common point does not change its voltage; it behaves like a virtual ground with a magnitude determined by the common-mode input voltages. The high-resistive emitter element does not play any role since it is shunted by the other low-resistive emitter follower. There is no negative feedback since the emitter voltage does not change at all when the input base voltages change. The common quiescent current vigorously steers between the two transistors and the output collector voltages vigorously change. The two transistors mutually ground their emitters; so, although they are common-collector stages, they actually act as common-emitter stages with maximum gain. Bias stability and independence from variations in device parameters can be improved by negative feedback introduced via cathode/emitter resistors with relatively small resistances.

Overdriven. If the input differential voltage changes significantly (more than about a hundred millivolts), the base-emitter junction of the transistor driven by the lower input voltage becomes backward biased and its collector voltage reaches the positive supply rail. The other transistor (driven by the higher input voltage) saturates and its collector voltage begins following the input one. This mode is used in differential switches and ECL gates.

Breakdown. If the input voltage continues increasing and exceeds the base-emitter breakdown voltage, the base-emitter junction of the transistor driven by the lower input voltage breaks down. If the input sources are low resistive, an unlimited current will flow directly through the "diode bridge" between the two input sources and will damage them.

At common mode, the emitter voltage follows the input voltage variations; there is a full negative feedback and the gain is minimum. At differential mode, the emitter voltage is fixed (equal to the instant common input voltage); there is no negative feedback and the gain is maximum.

CMRR

The **common-mode rejection ratio** (CMRR) of a differential amplifier (or other device) is the rejection by the device of unwanted input signals common to both input leads, relative to the wanted difference signal. An ideal differential amplifier would have infinite CMRR; this is not achievable in practice. A high CMRR is required when a differential signal must be amplified in the presence of a possibly large common-mode input. An example is audio transmission over balanced lines.

Theory

Ideally, a differential amplifier takes the voltages, $V_+$and V_-on its two inputs and produces an output voltage $V_\mathrm{o} = A_\mathrm{d}(V_+ - V_-)$, where $A_\mathrm{d}$is the differential gain. However, the output of a real differential amplifier is better described as

$$V_\mathrm{o} = A_\mathrm{d}(V_+ - V_-) + \tfrac{1}{2}A_\mathrm{cm}(V_+ + V_-),$$

where $A_\mathrm{cm}$is the common-mode gain, which is typically much smaller than the differential gain.

The CMRR is defined as the ratio of the powers of the differential gain over the common-mode gain, measured in positive decibels (thus using the 20 log rule):

$$\mathrm{CMRR} = \left(\frac{A_\mathrm{d}}{|A_\mathrm{cm}|}\right) = 10\log_{10}\left(\frac{A_\mathrm{d}}{A_\mathrm{cm}}\right)^2 dB = 20\log_{10}\left(\frac{A_\mathrm{d}}{|A_\mathrm{cm}|}\right) dB$$

As differential gain should exceed common-mode gain, this will be a positive number, and the higher the better.

The CMRR is a very important specification, as it indicates how much of the common-mode signal will appear in your measurement. The value of the CMRR often depends on signal frequency as well, and must be specified as a function thereof.

It is often important in reducing noise on transmission lines. For example, when measuring the resistance of a thermocouple in a noisy environment, the noise from the environment appears as an offset on both input leads, making it a common-mode voltage signal. The CMRR of the measurement instrument determines the attenuation applied to the offset or noise.

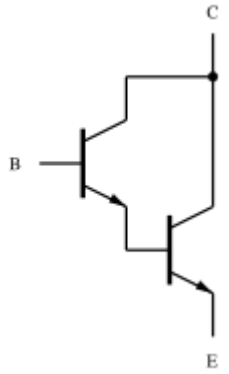
DARLINGTON AMPLIFIER

n electronics, the **Darlington transistor** (often called a **Darlington pair**) is a compound structure consisting of two bipolar transistors (either integrated or separated devices) connected in such a way that the current amplified by the first transistor is amplified further by the second one.[1] This configuration gives a much higher common/emitter current gain than each transistor taken separately and, in the case of integrated devices, can take less space than two individual transistors because they can use a shared collector. Integrated Darlington pairs come packaged singly in transistor-like

packages or as an array of devices (usually eight) in an integrated circuit.

The Darlington configuration was invented by Bell Laboratories engineer Sidney Darlington in 1953. He patented the idea of having two or three transistors on a single chip sharing a collector.[2]

A similar configuration but with transistors of opposite type (one NPN and one PNP) is the Sziklai pair, sometimes called the "complementary Darlington."



Behavior

View of the chip in an MJ1000

A Darlington pair is like a set of feeders with a high current gain (approximately the product of the gains of the two transistors). In fact, integrated devices have three leads (B, C and E), broadly equivalent to those of a standard transistor.

A general relation between the compound current gain and the individual gains is given by:

$$\beta_{\text{Darlington}} = \beta_1 \cdot \beta_2 + \beta_1 + \beta_2$$

If β_1 and β_2 are high enough (hundreds), this relation can be approximated with:

$$\beta_{\text{Darlington}} \approx \beta_1 \cdot \beta_2$$

Darlington pairs are available as integrated packages or can be made from two discrete transistors; Q_1 (the left-hand transistor in the diagram) can be a low power type, but normally Q_2 (on the right) will need to be high power. The maximum collector current I_C(max) of the pair is that of Q_2. A typical integrated power device is the 2N6282, which includes a switch-off resistor and has a current gain of 2400 at I_C=10A.

A Darlington pair can be sensitive enough to respond to the current passed by skin contact even at safe voltages. Thus it can form the input stage of a touch-sensitive switch.

A typical modern device has a current gain of 1000 or more, so that only a small base current is needed to make the pair switch on. However, this high current gain comes with several drawbacks.

Disadvantages

One drawback is an approximate doubling of the base/emitter voltage. Since there are two junctions between the base and emitter of the Darlington transistor, the equivalent base/emitter voltage is the sum of both base/emitter voltages:

$$V_{BE} = V_{BE1} + V_{BE2} \approx 2V_{BE1}$$

For silicon-based technology, where each V_{BEi} is about 0.65 V when the device is operating in the active or saturated region, the necessary base/emitter voltage of the pair is 1.3 V.

Another drawback of the Darlington pair is its increased "saturation" voltage. The output transistor is not allowed to saturate (i.e. its base-collector junction must remain reverse-biased) because the first

transistor, when saturated, establishes full (100%) parallel negative feedback between the collector and the base of the second transistor.[3] Since collector/emitter voltage is equal to the sum of its own base/emitter voltage and the collector-emitter voltage of the first transistor, both positive quantities in normal operation, it always exceeds the base-emitter voltage. (In symbols, $V_{CE2} = V_{CE1} + V_{BE2} > V_{BE2} \Rightarrow V_{C2} > V_{B2}$always.) Thus the "saturation" voltage of a Darlington transistor is one V_{BE} (about 0.65 V in silicon) higher than a single transistor saturation voltage, which is typically 0.1 - 0.2 V in silicon. For equal collector currents, this drawback translates to an increase in the dissipated power for the Darlington transistor over a single transistor. The increased low output level can cause troubles when TTL logic circuits are driven.

Another problem is a reduction in switching speed or response, because the first transistor cannot actively inhibit the base current of the second one, making the device slow to switch off. To alleviate this, the second transistor often has a resistor of a few hundred ohms connected between its base and emitter terminals.[1] This resistor provides a low impedance discharge path for the charge accumulated on the base-emitter junction, allowing a faster transistor turn-off.

The Darlington pair has more phase shift at high frequencies than a single transistor and hence can more easily become unstable with negative feedback (i.e., systems that use this configuration can have poor phase margin due to the extra transistor delay).

BOOTS STRAP

"Bootstrap" redirects here. For a UI web design tool called "Bootstrap", see Bootstrap (front-end framework).
For other uses, see Bootstrapping (disambiguation).

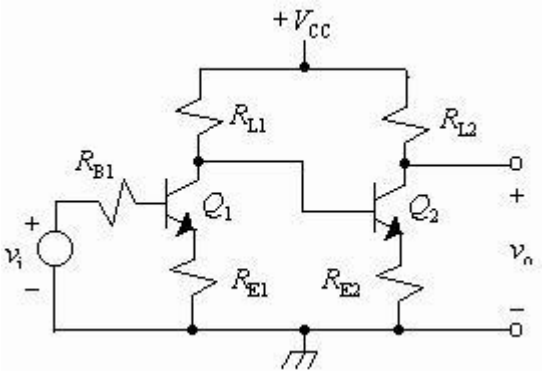
In general parlance, **bootstrapping** usually refers to the starting of a self-sustaining process that is supposed to proceed without external input. In computer technology the term (usually shortened to **booting**) usually refers to the process of loading the basic software into the memory of a computer after power-on or general reset, especially the

operating system which will then take care of loading other software as needed.

The term appears to have originated in the early 19th century United States (particularly in the phrase "pull oneself over a fence by one's bootstraps"), to mean an absurdly impossible action, an adynaton.[1][2][3]

Cascade amplifier

From Wikipedia, the free encyclopedia



Cascaded amplifier, a simplified diagram

A **cascade amplifier** is any two-port network constructed from a series of amplifiers, where each amplifier sends its output to the input of the next amplifier in a daisy chain.[1]

A cascade is basically a differential amplifier with one input grounded and the side with the real input has no load. It can also be seen as a common collector (emitter follower) followed by a common base. Since the input side has no load there is no gain on that side and the Miller effect does not come into play. In addition, Vds or Vce stays fairly constant which reduces distortion. Its advantage over the cascade is that it does not require as much voltage headroom. Its disadvantage is since it has two legs it requires twice as much current as a cascade for similar performance.

The complication in calculating the gain of cascaded stages is the non-ideal coupling between stages due to loading. Two cascaded common emitter stages are shown below. Because the input resistance

of the second stage forms a voltage divider with the output resistance of the first stage, the total gain is not the product of the individual (separated) stages.

Cascode

From Wikipedia, the free encyclopedia

The **cascode** is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer.

Compared to a single amplifier stage, this combination may have one or more of the following characteristics: higher input-output isolation, higher input impedance, high output impedance, higher gain or higher bandwidth.

In modern circuits, the cascode is often constructed from two transistors (BJTs or FETs), with one operating as a common emitter or common source and the other as a common base or common gate. The cascode improves input-output isolation (or reverse transmission) as there is no direct coupling from the output to input. This eliminates the Miller effect and thus contributes to a much higher bandwidth.

Operation

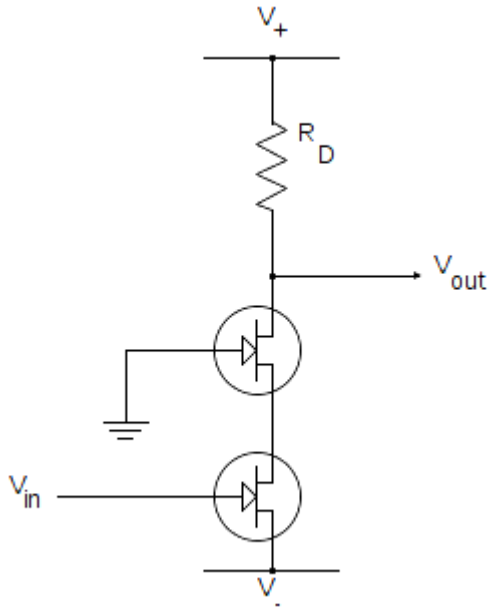


Figure 1: N-channel class A cascode amplifier

Figure 1 shows an example of cascode amplifier with a common source amplifier as input stage driven by signal source V_{in}. This input stage drives a common gate amplifier as output stage, with output signal V_{out}.

As the lower FET is conducting, by providing gate voltage, the upper FET conducts due to the potential difference now appearing between its gate and source.

The major advantage of this circuit arrangement stems from the placement of the upper field-effect transistor (FET) as the load of the input (lower) FET's output terminal (drain). Because at operating frequencies the upper FET's gate is effectively grounded, the upper FET's source voltage (and therefore the input transistor's drain) is held at nearly constant voltage during operation. In other words, the upper FET exhibits a low input resistance to the lower FET, making the voltage gain of the lower FET very small, which dramatically reduces the Miller feedback capacitance from the lower FET's drain to gate. This loss of voltage gain is recovered by the upper FET. Thus, the upper transistor permits the lower FET to operate with minimum negative (Miller) feedback, improving its bandwidth.

The upper FET gate is electrically grounded, so charge and discharge of stray capacitance C_{dg} between drain and gate is simply through R_D and the output load (say R_{out}), and the frequency response is affected only for frequencies above the associated RC time constant: $\tau = C_{dg}\ R_D//R_{out}$, namely $f = 1/(2\pi\tau)$, a rather high frequency because C_{dg} is small. That is, the upper FET gate does not suffer from Miller amplification of C_{dg}.

If the upper FET stage were operated alone using its source as input node (i.e. common gate (CG) configuration), it would have good voltage gain and wide bandwidth. However, its low input impedance would limit its usefulness to very low impedance voltage drivers. Adding the lower FET results in a high input impedance, allowing the cascode stage to be driven by a high impedance source.

If one were to replace the upper FET with a typical inductive/resistive load, and take the output from the input transistor's drain (i.e. a

common source(CS) configuration), the CS configuration would offer the same input impedance as the cascode, but the cascode configuration would offer a potentially greater gain and much greater bandwidth.

Stability

The cascode arrangement is also very stable. Its output is effectively isolated from the input both electrically and physically. The lower transistor has nearly constant voltage at both drain and source and thus there is essentially "nothing" to feed back into its gate. The upper transistor has nearly constant voltage at its gate and source. Thus, the only nodes with significant voltage on them are the input and output, and these are separated by the central connection of nearly constant voltage and by the physical distance of two transistors. Thus in practice there is little feedback from the output to the input. Metal shielding is both effective and easy to provide between the two transistors for even greater isolation when required. This would be difficult in one-transistor amplifier circuits, which at high frequencies would require neutralization.

Biasing

As shown, the cascode circuit using two "stacked" FETs imposes some restrictions on the two FETs — namely, the upper FET must be biased so its source voltage is high enough (the lower FET drain voltage may swing too low, causing it to saturate). Insurance of this condition for FETs requires careful selection for the pair, or special biasing of the upper FET gate, increasing cost.

The cascode circuit can also be built using bipolar transistors, or MOSFETs, or even one FET (or MOSFET) and one BJT. In the latter case, the BJT must be the upper transistor; otherwise, the (lower) BJT will always saturate[citation needed] unless extraordinary steps are taken to bias it.

Advantages

The cascode arrangement offers high gain, high bandwidth, high slew rate, high stability, and high input impedance. The parts count is very low for a two-transistor circuit.

Disadvantages

The cascode circuit requires two transistors and requires a relatively high supply voltage. For the two-FET cascode, both transistors must be biased with ample V_{DS} in operation, imposing a lower limit on the supply voltage.

UNIT-3 JFET AND MOSFET AMPLIFIERS

ANALYSIS OF JFET

Small-signal modeling is a common analysis technique in electrical engineering which is used to approximate the behavior of nonlinear devices with linear equations. This linearization is formed about the DC bias point of the device (that is, the voltage/current levels present when no signal is applied), and can be accurate for small excursions about this point.

Motivation

Many electronic circuits, such as radio receivers, communications, and signal processing circuits, generally carry small time-varying (AC) signals on top of a constant (DC) bias. This suggests using a method akin to approximation by finite difference method to analyze relatively small perturbations about the bias point.

Any nonlinear device which can be described quantitatively using a formula can then be 'linearized' about a bias point by taking partial derivatives of the formula with respect to all governing variables. These partial derivatives can be associated with physical quantities (such as capacitance, resistance and inductance), and a circuit diagram relating them can be formulated. Small-signal models exist for electron tubes, diodes, field-effect transistors (FET) and bipolar transistors, notably the hybrid-pi model and various two-port networks.

Variable notation

- Large-signal DC quantities are denoted by uppercase letters with uppercase subscripts. For example, the DC input bias voltage of a transistor would be denoted V_{IN}.
- Small-signal quantities are denoted using lowercase letters with lowercase subscripts. For example, the input signal of a transistor would be denoted as v_{in}.

- Total quantities, combining both small-signal and large-signal quantities, are denoted using lower case letters and uppercase subscripts. For example, the total input voltage to the aforementioned transistor would be $v_{\mathrm{IN}}(t) = V_{\mathrm{IN}} + v_{\mathrm{in}}(t)$.

Example: PN junction diodes

Main article: Diode modelling § Small-signal modelling

The (large-signal) Shockley equation for a diode can be linearized about the bias point or quiescent point (sometimes called Q-point) to find the small-signal conductance, capacitance and resistance of the diode. This procedure is described in more detail under diode modeling, which provides an example of the linearization procedure followed in all small-signal models of semiconductor devices.

Differences between small signal and large signal

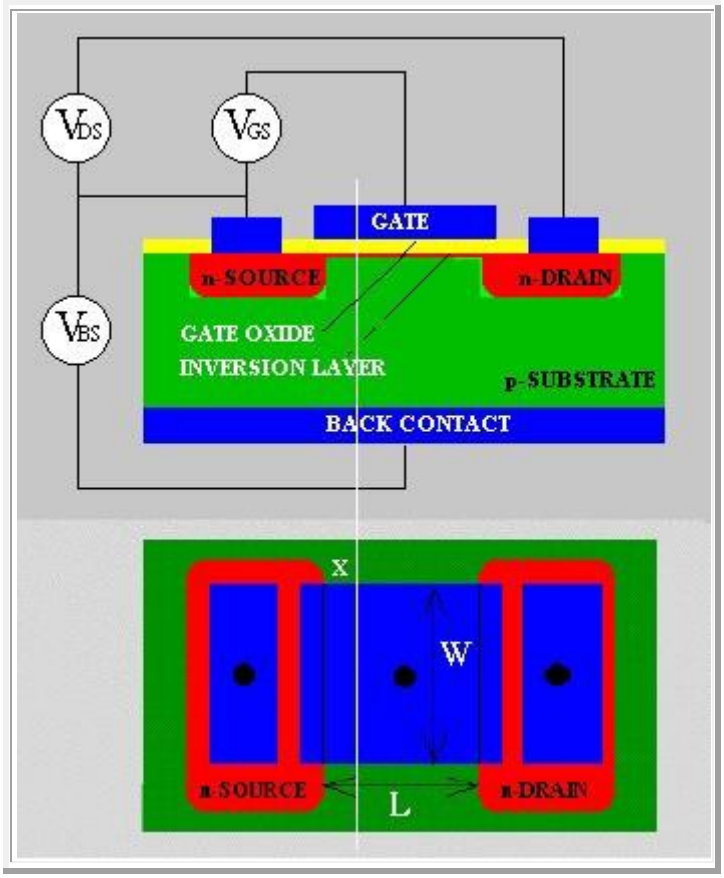
A large signal is a DC signal (or an AC signal at a point in time) that is one or more orders of magnitude larger than the small signal and is used to analyse a circuit containing non-linear components and calculate an operating point (bias) of these components.

A small signal is an AC signal superimposed on a circuit containing a large signal.

In analysis of the small signal's contribution to the circuit, the non-linear components are modeled as linear components

ANALYSIS OF MOSFET AMP

From this relationship, lets now "derive" the all important characteristic relating drain current and drain-source voltage. Consider the following configuration:



At some position x along the source-drain channel:

$$(\text{current in channel at x}) = (\text{mobility})\,(\text{electric charge at x})\,(\text{electric field at x})$$

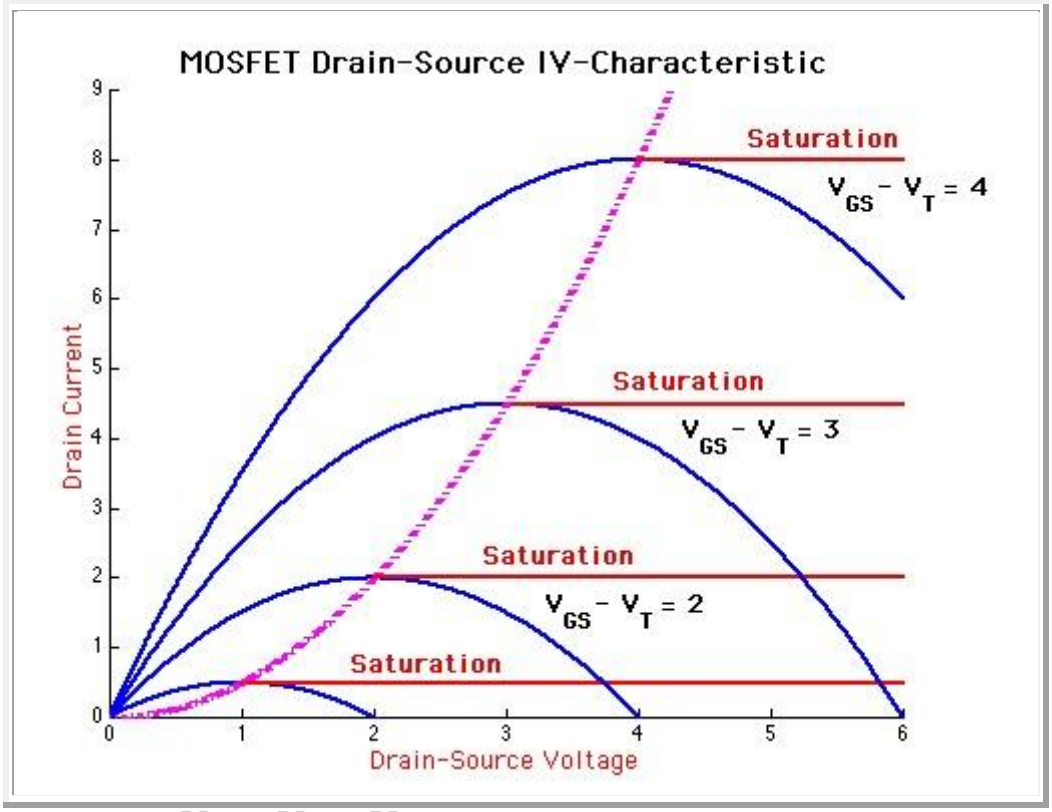
$$I_D(x) = \mu\, Q_{inv}(x)\left(-\frac{d\,V_x}{d\,x}\right)$$

$$= \mu\, C_{ox}\, W\left(V_G - V_S - V_x - V_T\right)\frac{d\,V_x}{d\,x}$$

$$\int_0^L I_D(x)\,d\,x = \int_0^{V_{DS}} \mu\, C_{ox}\, W\left(V_G - V_S - V_x - V_T\right)d\,V_x$$

But since I_D is constant throughout conducting channel:

$$I_D = \mu\, C_{ox}\,\frac{W}{L}\left\{\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}{V_{DS}}^2\right\}$$



At the peak $V_{GS} = V_{DS} + V_T$ so that stored charge at the drain vanishes and the equation is no longer valid. At this point the drain current has reached its "saturation" value as indicated in the figure above. The drain current at maximum follows the parabolic equation

$$I_D = \mu C_{ox} \frac{W}{2L} V_{DS}^2$$

.

COMMON SOURCE

Common source

From Wikipedia, the free encyclopedia

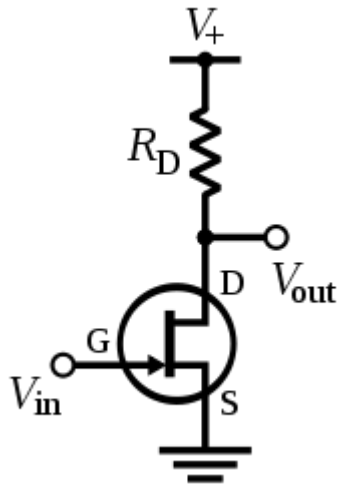


Figure 1: Basic N-channel JFET common-source circuit (neglecting biasing details).

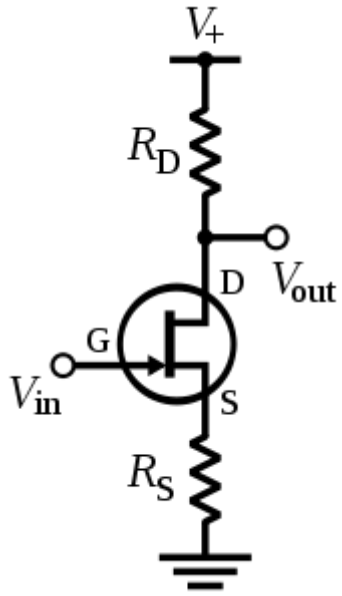


Figure 2: Basic N-channel JFET common-source circuit with source degeneration.

In electronics, a **common-source** amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the

source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit is the common-emitter amplifier.

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. (See classification of amplifiers). As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics. The CS–CG combination is called a cascode amplifier.

Characteristics

At low frequencies and using a simplified hybrid-pi model, the following small-signal characteristics can be derived.

	Definition	Expression
Current gain	$A_\mathrm{i} \triangleq \frac{i_\mathrm{out}}{i_\mathrm{in}}$	∞
Voltage gain	$A_\mathrm{v} \triangleq \frac{v_\mathrm{out}}{v_\mathrm{in}}$	$-\frac{g_\mathrm{m} R_\mathrm{D}}{1+g_\mathrm{m} R_\mathrm{S}}$
Input impedance	$r_\mathrm{in} \triangleq \frac{v_\mathrm{in}}{i_\mathrm{in}}$	∞
Output impedance	$r_\mathrm{out} \triangleq \frac{v_\mathrm{out}}{i_\mathrm{out}}$	R_D

Bandwidth

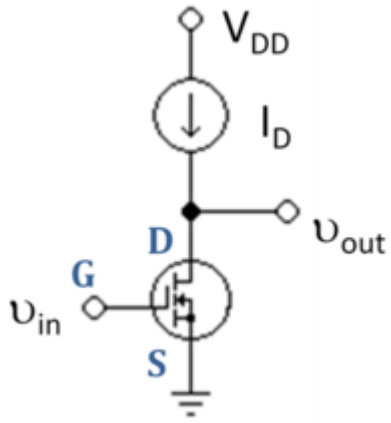


Figure 3: Basic N-channel MOSFET common-source amplifier with active load I_D.

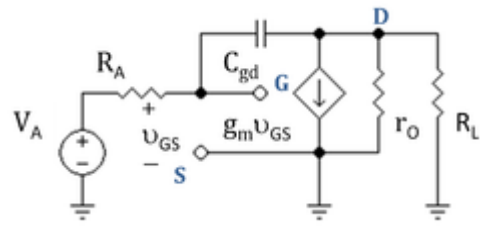


Figure 4: Small-signal circuit for N-channel MOSFET common-source amplifier.

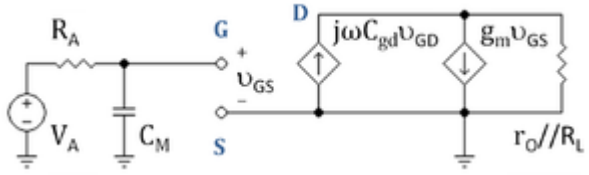


Figure 5: Small-signal circuit for N-channel MOSFET common-source amplifier using Miller's theorem to introduce Miller capacitance C_M.

The bandwidth of the common-source amplifier tends to be low, due to high capacitance resulting from the Miller effect. The gate-drain capacitance is effectively multiplied by the factor $1 + |A_v|$, thus

increasing the total input capacitance and lowering the overall bandwidth.

Figure 3 shows a MOSFET common-source amplifier with an active load. Figure 4 shows the corresponding small-signal circuit when a load resistor R_L is added at the output node and a Thévenin driver of applied voltage V_A and series resistance R_A is added at the input node. The limitation on bandwidth in this circuit stems from the coupling of parasitic transistor capacitance C_{gd} between gate and drain and the series resistance of the source R_A. (There are other parasitic capacitances, but they are neglected here as they have only a secondary effect on bandwidth.)

Using Miller's theorem, the circuit of Figure 4 is transformed to that of Figure 5, which shows the Miller capacitance C_M on the input side of the circuit. The size of C_M is decided by equating the current in the input circuit of Figure 5 through the Miller capacitance, say i_M, which is:

$$i_{\mathrm{M}} = j\omega C_{\mathrm{M}} v_{\mathrm{GS}} = j\omega C_{\mathrm{M}} v_{\mathrm{G}},$$

to the current drawn from the input by capacitor C_{gd} in Figure 4, namely $j\omega C_{gd}\, v_{GD}$. These two currents are the same, making the two circuits have the same input behavior, provided the Miller capacitance is given by:

$$C_{\mathrm{M}} = C_{\mathrm{gd}} \frac{v_{\mathrm{GD}}}{v_{\mathrm{GS}}} = C_{\mathrm{gd}} \left(1 - \frac{v_{\mathrm{D}}}{v_{\mathrm{G}}}\right).$$

Usually the frequency dependence of the gain v_D / v_G is unimportant for frequencies even somewhat above the corner frequency of the amplifier, which means a low-frequency hybrid-pi model is accurate for determining v_D / v_G. This evaluation is Miller's approximation[1] and provides the estimate (just set the capacitances to zero in Figure 5):

$$\frac{v_{\mathrm{D}}}{v_{\mathrm{G}}} \approx -g_{\mathrm{m}}(r_{\mathrm{O}} \| R_{\mathrm{L}}),$$

so the Miller capacitance is

$$C_{\mathrm{M}} = C_{\mathrm{gd}}\,(1 + g_{\mathrm{m}}(r_{\mathrm{O}} \| R_{\mathrm{L}})).$$

The gain g_m ($r_O \parallel R_L$) is large for large R_L, so even a small parasitic capacitance C_{gd} can become a large influence in the frequency response of the amplifier, and many circuit tricks are used to counteract this effect. One trick is to add a common-gate (current-follower) stage to make a cascode circuit. The current-follower stage presents a load to the common-source stage that is very small, namely the input resistance of the current follower ($R_L \approx 1 / g_m \approx V_{ov} / (2I_D)$; see common gate). Small R_L reduces C_M.[2] The article on the common-emitter amplifier discusses other solutions to this problem.

Returning to Figure 5, the gate voltage is related to the input signal by voltage division as:

$$v_{\mathrm{G}} = V_{\mathrm{A}} \frac{1/(j\omega C_{\mathrm{M}})}{1/(j\omega C_{\mathrm{M}}) + R_{\mathrm{A}}} = V_{\mathrm{A}} \frac{1}{1 + j\omega C_{\mathrm{M}} R_{\mathrm{A}}}.$$

The bandwidth (also called the 3dB frequency) is the frequency where the signal drops to $1/\sqrt{2}$ of its low-frequency value. (In decibels, $\mathrm{dB}(\sqrt{2}) = 3.01$ dB). A reduction to $1/\sqrt{2}$ occurs when $\omega C_M R_A = 1$, making the input signal at this value of ω (call this value ω_{3dB}, say) $v_G = V_A / (1+j)$. The magnitude of $(1+j) = \sqrt{2}$. As a result the 3dB frequency $f_{3dB} = \omega_{3dB} / (2\pi)$ is:

$$f_{3\mathrm{dB}} = \frac{1}{2\pi R_{\mathrm{A}} C_{\mathrm{M}}} = \frac{1}{2\pi R_{\mathrm{A}} [C_{\mathrm{gd}}(1 + g_{\mathrm{m}}(r_{\mathrm{O}} \| R_{\mathrm{L}})]}.$$

If the parasitic gate-to-source capacitance C_{gs} is included in the analysis, it simply is parallel with C_M, so

$$f_{3\mathrm{dB}} = \frac{1}{2\pi R_{\mathrm{A}} (C_{\mathrm{M}} + C_{\mathrm{gs}})} = \frac{1}{2\pi R_{\mathrm{A}} [C_{\mathrm{gs}} + C_{\mathrm{gd}}(1 + g_{\mathrm{m}}(r_{\mathrm{O}} \| R_{\mathrm{L}}))]}.$$

Notice that f_{3dB} becomes large if the source resistance R_A is small, so the Miller amplification of the capacitance has little effect upon the bandwidth for small R_A. This observation suggests another circuit

trick to increase bandwidth: add a common-drain (voltage-follower) stage between the driver and the common-source stage so the Thévenin resistance of the combined driver plus voltage follower is less than the R_A of the original driver.[3]

Examination of the output side of the circuit in Figure 2 enables the frequency dependence of the gain v_D / v_G to be found, providing a check that the low-frequency evaluation of the Miller capacitance is adequate for frequencies f even larger than f_{3dB}. (See article on pole splitting to see how the output side of the circuit is handled.)

COMMON GATE

Common gate

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This article includes a list of references, but **its sources remain unclear because it has insufficient inline citations**. Please help to improve this article by introducing more precise citations. (April 2009)

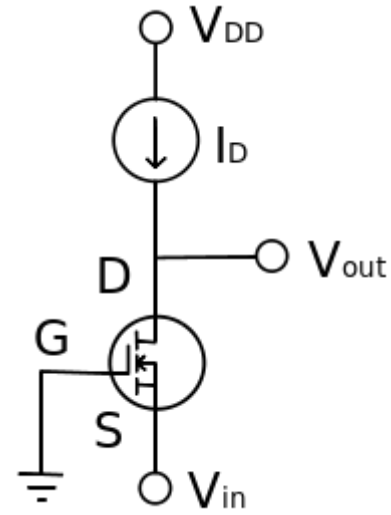


Figure 1: Basic N-channel common-gate circuit (neglecting biasing details); current source I_D represents an active load; signal is applied

at node V_{in} and output is taken from node V_{out}; output can be current or voltage

In electronics, a **common-gate** amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a current buffer or voltage amplifier. In this circuit the source terminal of the transistor serves as the input, the drain is the output and the gate is connected to ground, or "common," hence its name. The analogous bipolar junction transistor circuit is the common-base amplifier.

Applications

This configuration is used less often than the common source or source follower. It is useful in, for example, CMOS RF receivers, especially when operating near the frequency limitations of the FETs; it is desirable because of the ease of impedance matching and potentially has lower noise. Gray and Meyer[1] provide a general reference for this circuit.

Low-frequency characteristics

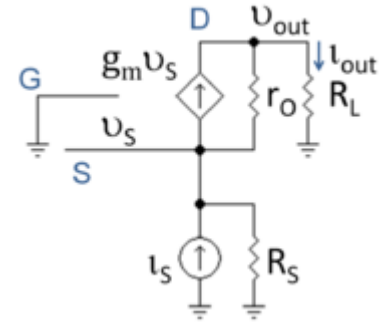


Figure 2: Small-signal low-frequency hybrid-pi model for amplifier driven by a Norton signal source

At low frequencies and under small-signal conditions, the circuit in Figure 1 can be represented by that in Figure 2, where the hybrid-pi model for the MOSFET has been employed.

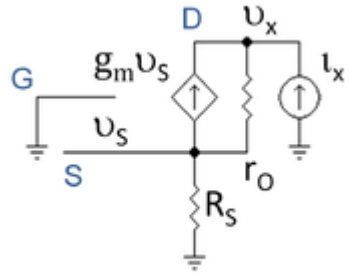


Figure 3: Hybrid pi model with test source i_x at output to find output resistance

The amplifier characteristics are summarized below in Table 1. The approximate expressions use the assumptions (usually accurate) $r_O >> R_L$ and $g_m r_O >> 1$.

Table 1	**Definition**	**Expression**	**Approximate expression**
Short-circuit current gain	$A_i = \left.\frac{i_{\text{out}}}{i_S}\right\|_{R_L=0}$	1	1
Open-circuit voltage gain	$A_v = \left.\frac{v_{\text{out}}}{v_S}\right\|_{R_L=\infty}$	$((g_m + g_{mb})r_O + 1)\frac{R_L}{r_O + R_L}$	$g_m R_L$
Input resistance	$R_{\text{in}} = \frac{v_S}{i_S}$	$\frac{R_L + r_O}{(g_m + g_{mb})r_O + 1}$	$\frac{1}{g_m}$
Output resistance	$R_{\text{out}} = \frac{v_x}{i_x}$	$(1 + (g_m + g_{mb})r_O)R_S + r_O \, r_O$	

Note: Parallel lines (||) indicate components in parallel.

In general the overall voltage/current gain may be substantially less than the open/short circuit gains listed above (depending on the source and load resistances) due to the loading effect.

Closed circuit voltage gain

Taking input and output loading into consideration, the closed circuit voltage gain (that is, the gain with load R_L and source with resistance R_S both attached) of the common gate can be written as:

$$A_\mathrm{v} \approx \frac{g_m R_\mathrm{L}}{1+g_m R_S},$$

which has the simple limiting forms

$$A_\mathrm{v} = \frac{R_L}{R_S} \quad \text{or} \quad A_\mathrm{v} = g_m R_L,$$

depending upon whether $g_m R_S$ is much larger or much smaller than one.

In the first case the circuit acts as a current follower, as understood as follows: for $R_S >> 1/g_m$ the voltage source can be replaced by its Norton equivalent with Norton current $v_{Thév} / R_S$ and parallel Norton resistance R_S. Because the amplifier input resistance is small, the driver delivers by current division a current $v_{Thév} / R_S$ to the amplifier. The current gain is unity, so the same current is delivered to the output load R_L, producing by Ohm's law an output voltage $v_{out} = v_{Thév} R_L / R_S$, that is, the first form of the voltage gain above.

In the second case $R_S << 1/g_m$ and the Thévenin representation of the source is useful, producing the second form for the gain, typical of voltage amplifiers.

Because the input impedance of the common-gate amplifier is very low, the cascode amplifier often is used instead. The cascode places a common-source amplifier between the voltage driver and the common-gate circuit to permit voltage amplification using a driver with $R_S >> 1/g_m$.

JFET SOURCE FOLLOWER

The Common Source JFET Amplifier

So far we have looked at the bipolar type transistor amplifier and especially the common emitter amplifier, but small signal amplifiers can also be made using **Field Effect Transistors** or **FET's** for short. These devices have the advantage over bipolar transistors of having an extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals.

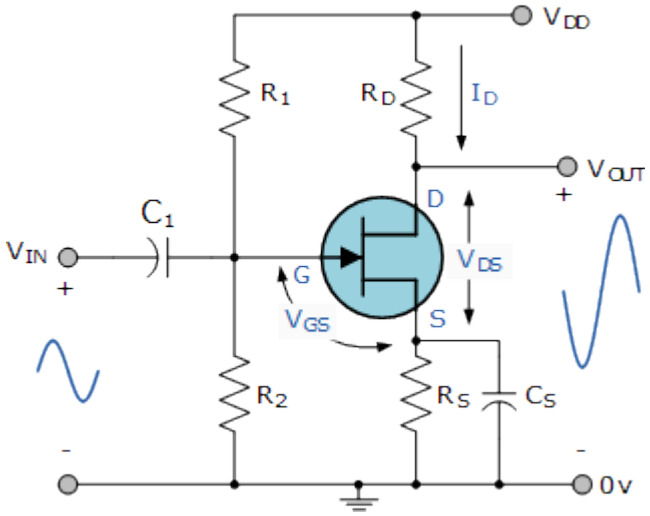
The design of an amplifier circuit based around a junction field effect transistor or "JFET", (N-channel FET for this tutorial) or even a metal oxide silicon FET or "MOSFET" is exactly the same principle as that for the bipolar transistor circuit used for a Class A amplifier circuit we looked at in the previous tutorial.

Firstly, a suitable quiescent point or "Q-point" needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices.

These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors. In this tutorial about FET amplifiers we will look at the popular **Common Source JFET Amplifier** as this is the most widely used JFET amplifier design.

Consider the Common Source JFET Amplifier circuit configuration below.

Common Source JFET Amplifier



The amplifier circuit consists of an N-channel JFET, but the device could also be an equivalent N-channel depletion-mode MOSFET as the circuit diagram would be the same just a change in the FET, connected in a common source configuration. The JFET gate voltage Vg is biased through the potential divider network set up by resistors R1 and R2 and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor.

Unlike a bipolar transistor circuit, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required. We can compare the JFET to the bipolar junction transistor (BJT) in the following table.

JFET to BJT Comparison

Junction FET	Bipolar Transistor
Gate, (G)	Base, (B)
Drain, (D)	Collector, (C)
Source, (S)	Emitter, (E)
Gate Supply, (V_G)	Base Supply, (V_B)

Drain Supply, (V_{DD})	Collector Supply, (V_{CC})
Drain Current, (I_D)	Collector Current, (I_C)

Since the N-Channel JFET is a depletion mode device and is normally "ON", a negative gate voltage with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self biasing arrangement as long as a steady current flows through the JFET even when there is no input signal present and Vg maintains a reverse bias of the gate-source pn junction.

In our simple example, the biasing is provided from a potential divider network allowing the input signal to produce a voltage fall at the gate as well as voltage rise at the gate with a sinusoidal signal. Any suitable pair of resistor values in the correct proportions would produce the correct biasing voltage so the DC gate biasing voltage Vg is given as:

$$V_G = \frac{V_{DD}\,R_2}{R_1 + R_2} = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Note that this equation only determines the ratio of the resistors R1 and R2, but in order to take advantage of the very high input impedance of the JFET as well as reducing the power dissipation within the circuit, we need to make these resistor values as high as possible, with values in the order of 1 to 10MΩ being common.

The input signal, (Vin) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage Vg applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, Rd. The output voltage, Vout is developed across this load resistance. The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, Rs

included in the source lead with the same drain current flowing through this resistor. Resistor, Rs is also used to set the JFET amplifiers “Q-point”.

When the JFET is switched fully “ON” a voltage drop equal to Rs x Id is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across Rs due to the drain current provides the necessary reverse biasing condition across the gate resistor, R2 effectively generating negative feedback.

So in order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, Vg. This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, Id is also equal to the Source current, Is as “No Current” enters the Gate terminal and this can be given as:

$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

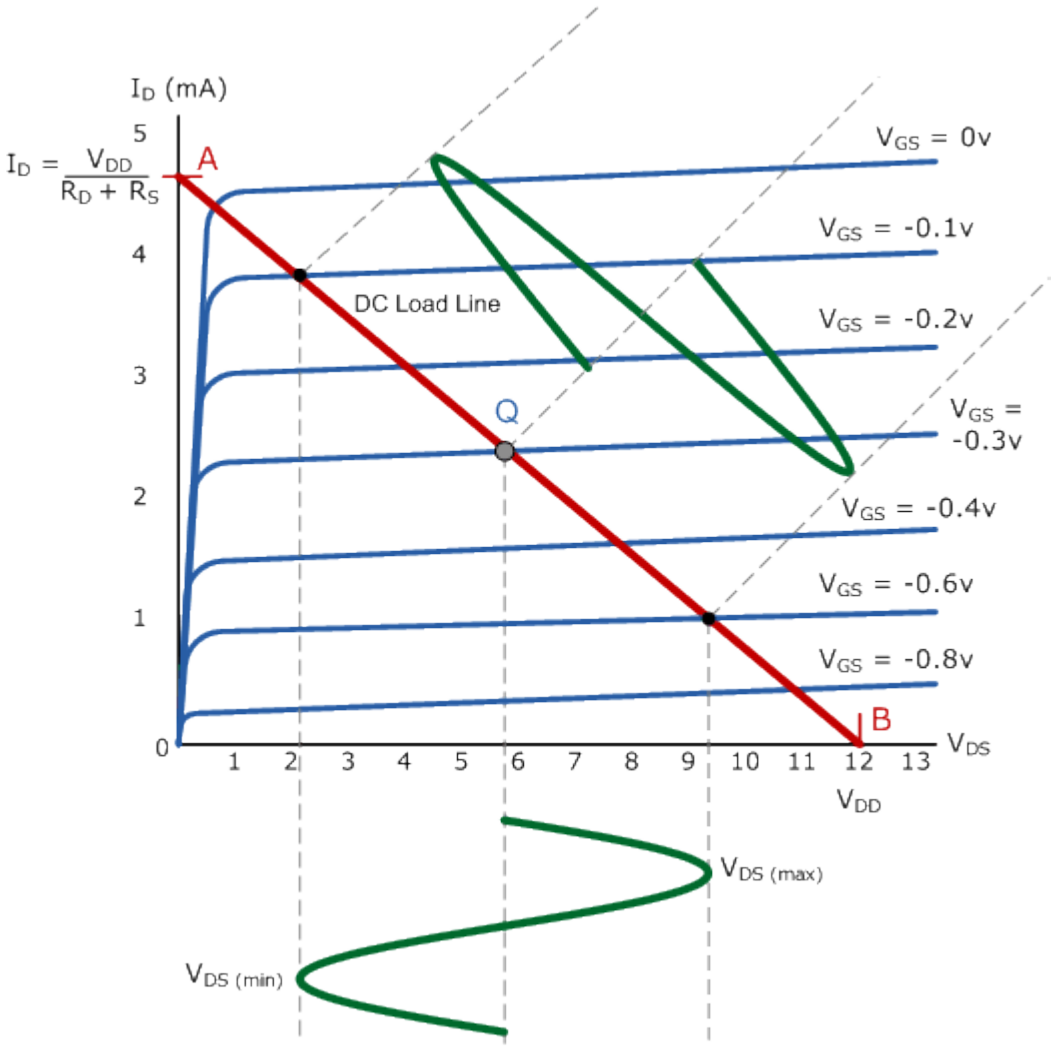
This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistor, Rs and the source by-pass capacitor, Cs serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped across Rs.

The the value in farads of the source by-pass capacitor is generally fairly high above 100uF and will be polarized. This gives the

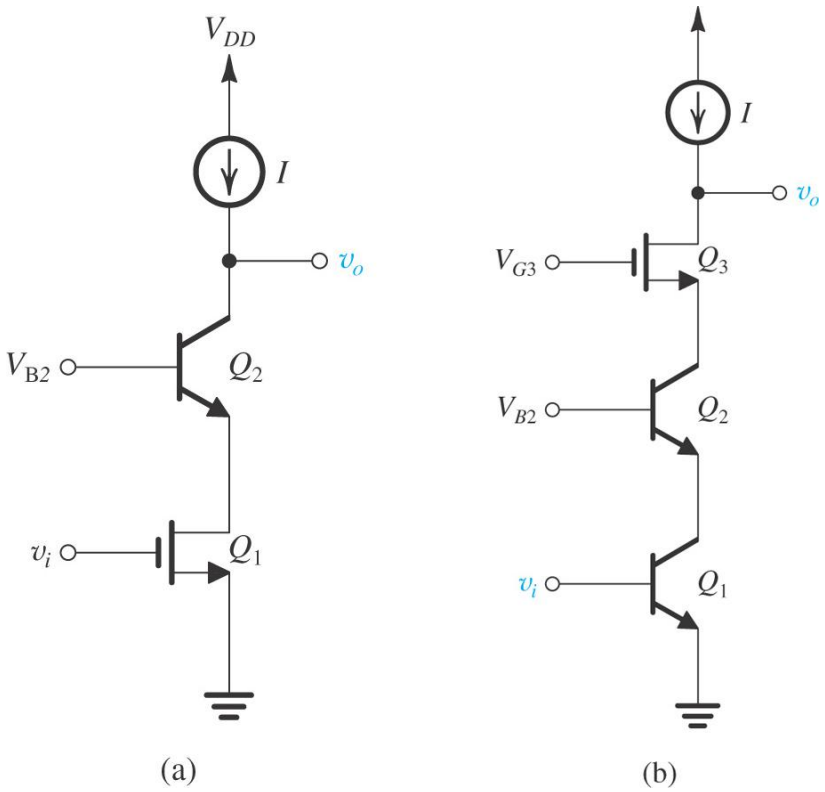
capacitor an impedance value much smaller, less than 10% of the transconductance, gm (the transfer coefficient representing gain) value of the device. At high frequencies the by-pass capacitor acts essentially as a short-circuit and the source will be effectively connected directly to ground.

The basic circuit and characteristics of a **Common Source JFET Amplifier** are very similar to that of the common emitter amplifier. A DC load line is constructed by joining the two points relating to the drain current, Id and the supply voltage, Vdd remembering that when Id = 0: (Vdd = Vds) and when Vds = 0: (Id = Vdd/R_L). The load line is therefore the intersection of the curves at the Q-point as follows.

Common Source JFET Amplifier Characteristics Curves



BiCMOS Cascode



UNIT-4 FREQUENCY ANALYSIS OF BJT AND MOSFET AMPLIFIERS

LOW FREQUENCY AND MILLER EFFECT

Miller effect

From Wikipedia, the free encyclopedia

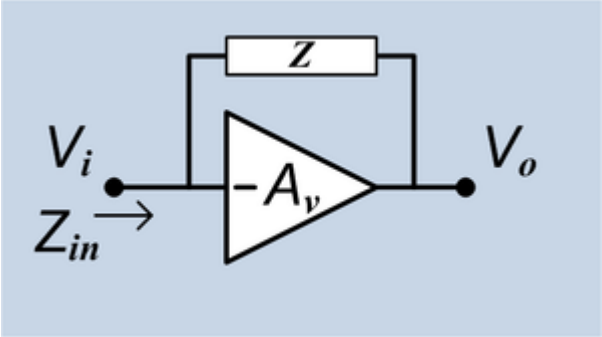
In electronics, the **Miller effect** accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals. The virtually increased input capacitance due to the Miller effect is given by

$$C_M = C(1 + A_v)$$

where $-A_v$is the gain of the amplifier and C is the feedback capacitance.

Although the term Miller effect normally refers to capacitance, any impedance connected between the input and another node exhibiting gain can modify the amplifier input impedance via this effect. These properties of the Miller effect are generalized in the Miller theorem. The Miller capacitance due to parasitic capacitance between the output and input of active devices like transistors and vacuum tubes is a major factor limiting their gain at high frequencies. Miller capacitance was identified in 1920 in triode vacuum tubes by John Milton Miller.

Derivation



An ideal voltage inverting amplifier with an impedance connecting output to input.

Consider an ideal inverting voltage amplifier of gain $-A_v$with an impedance Zconnected between its input and output nodes. The output voltage is therefore $V_o = -A_v V_i$. Assuming that the amplifier input draws no current, all of the input current flows through Z, and is therefore given by

$$I_i = \frac{V_i - V_o}{Z} = \frac{V_i(1 + A_v)}{Z}.$$

The input impedance of the circuit is

$$Z_{in} = \frac{V_i}{I_i} = \frac{Z}{1 + A_v}.$$

If Z represents a capacitor with impedance $Z = \frac{1}{sC}$, the resulting input impedance is

$$Z_{in} = \frac{1}{sC_M} \quad \text{where} \quad C_M = C(1 + A_v).$$

Thus the effective or **Miller capacitance** C_M is the physical C multiplied by the factor $(1 + A_v)$.[2]

Effects

As most amplifiers are inverting (A_v as defined above is positive), the effective capacitance at their inputs is increased due to the Miller effect. This can reduce the bandwidth of the amplifier, restricting its range of operation to lower frequencies. The tiny junction and stray capacitances between the base and collector terminals of a Darlington transistor, for example, may be drastically increased by the Miller effects due to its high gain, lowering the high frequency response of the device.

It is also important to note that the Miller capacitance is the capacitance seen looking into the input. If looking for all of the RC time constants (poles) it is important to include as well the capacitance seen by the output. The capacitance on the output is often neglected since it sees $C(1 + 1/A_v)$and amplifier outputs are typically low impedance. However if the amplifier has a high impedance output, such as if a gain stage is also the output stage, then this RC can have a significant impact on the performance of the amplifier. This is when pole splitting techniques are used.

The Miller effect may also be exploited to synthesize larger capacitors from smaller ones. One such example is in the stabilization of feedback amplifiers, where the required capacitance may be too large to practically include in the circuit. This may be particularly important in the design of integrated circuits, where capacitors can consume significant area, increasing costs.

Mitigation

The Miller effect may be undesired in many cases, and approaches may be sought to lower its impact. Several such techniques are used in the design of amplifiers.

A current buffer stage may be added at the output to lower the gain A_v between the input and output terminals of the amplifier (though not necessarily the overall gain). For example, a common base may be used as a current buffer at the output of a common emitter stage,

forming a cascode. This will typically reduce the Miller effect and increase the bandwidth of the amplifier.

Alternatively, a voltage buffer may be used before the amplifier input, reducing the effective source impedance seen by the input terminals. This lowers the RC time constant of the circuit and typically increases the bandwidth.

Impact on frequency response

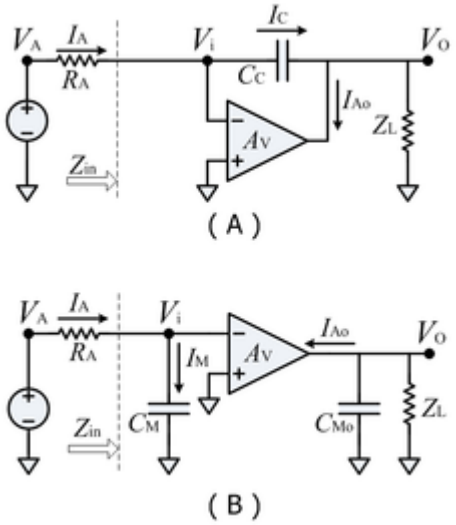


Figure 2: Amplifier with feedback capacitor C_C.

Figure 2A shows an example of Figure 1 where the impedance coupling the input to the output is the coupling capacitor C_C. A Thévenin voltage source V_A drives the circuit with Thévenin resistance R_A. The output impedance of the amplifier is considered low enough that the relationship $V_o = A_v V_i$ is presumed to hold. At the output Z_L serves as the load. (The load is irrelevant to this discussion: it just provides a path for the current to leave the circuit.) In Figure 2A, the coupling capacitor delivers a current $j\omega C_C(V_i - V_o)$ to the output node.

Figure 2B shows a circuit electrically identical to Figure 2A using Miller's theorem. The coupling capacitor is replaced on the input side of the circuit by the Miller capacitance C_M, which draws the same

current from the driver as the coupling capacitor in Figure 2A. Therefore, the driver sees exactly the same loading in both circuits. On the output side, a capacitor $C_{Mo} = (1 + 1/A_v)C_C$ draws the same current from the output as does the coupling capacitor in Figure 2A.

In order that the Miller capacitance draw the same current in Figure 2B as the coupling capacitor in Figure 2A, the Miller transformation is used to relate C_M to C_C. In this example, this transformation is equivalent to setting the currents equal, that is

$$j\omega C_C(V_i - V_O) = j\omega C_M V_i,$$

or, rearranging this equation

$$C_M = C_C\left(1 - \frac{V_o}{V_i}\right) = C_C(1 + A_v).$$

This result is the same as C_M of the Derivation Section.

The present example with A_v frequency independent shows the implications of the Miller effect, and therefore of C_C, upon the frequency response of this circuit, and is typical of the impact of the Miller effect (see, for example, common source). If $C_C = 0$ F, the output voltage of the circuit is simply $A_v\ v_A$, independent of frequency. However, when C_C is not zero, Figure 2B shows the large Miller capacitance appears at the input of the circuit. The voltage output of the circuit now becomes

$$V_o = -A_v V_i = -A_v \frac{V_A}{1 + j\omega C_M R_A},$$

and rolls off with frequency once frequency is high enough that $\omega C_M R_A \geq 1$. It is a low-pass filter. In analog amplifiers this curtailment of frequency response is a major implication of the Miller effect. In this example, the frequency ω_{3dB} such that $\omega_{3dB} C_M R_A = 1$ marks the end of the low-frequency response region and sets the bandwidth or cutoff frequency of the amplifier.

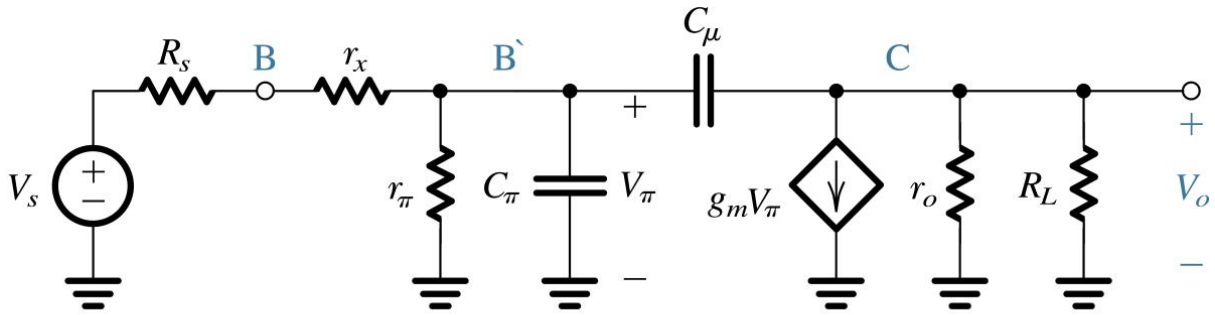
The effect of C_M upon the amplifier bandwidth is greatly reduced for low impedance drivers ($C_M R_A$ is small if R_A is small). Consequently, one way to minimize the Miller effect upon bandwidth is to use a low-impedance driver, for example, by interposing a voltage follower stage between the driver and the amplifier, which reduces the apparent driver impedance seen by the amplifier.

The output voltage of this simple circuit is always $A_v v_i$. However, real amplifiers have output resistance. If the amplifier output resistance is included in the analysis, the output voltage exhibits a more complex frequency response and the impact of the frequency-dependent current source on the output side must be taken into account.[3] Ordinarily these effects show up only at frequencies much higher than the roll-off due to the Miller capacitance, so the analysis presented here is adequate to determine the useful frequency range of an amplifier dominated by the Miller effect.

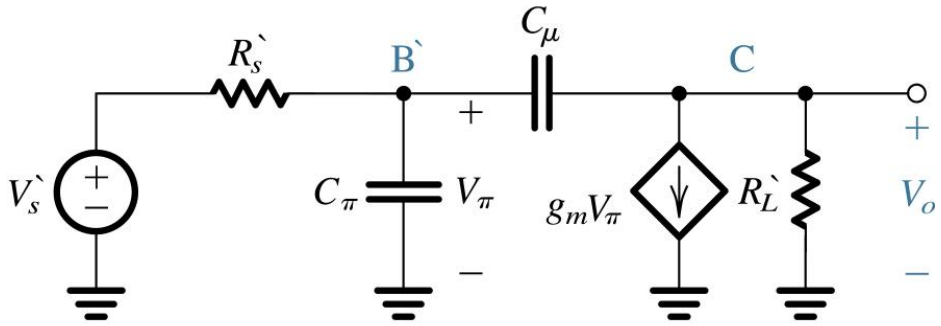
Miller approximation

This example also assumes A_v is frequency independent, but more generally there is frequency dependence of the amplifier contained implicitly in A_v. Such frequency dependence of A_v also makes the Miller capacitance frequency dependent, so interpretation of C_M as a capacitance becomes more difficult. However, ordinarily any frequency dependence of A_v arises only at frequencies much higher than the roll-off with frequency caused by the Miller effect, so for frequencies up to the Miller-effect roll-off of the gain, A_v is accurately approximated by its low-frequency value. Determination of C_M using A_v at low frequencies is the so-called **Miller approximation**.[2] With the Miller approximation, C_M becomes frequency independent, and its interpretation as a capacitance at low frequencies is secure.

CE Amplifier – High Frequency Response



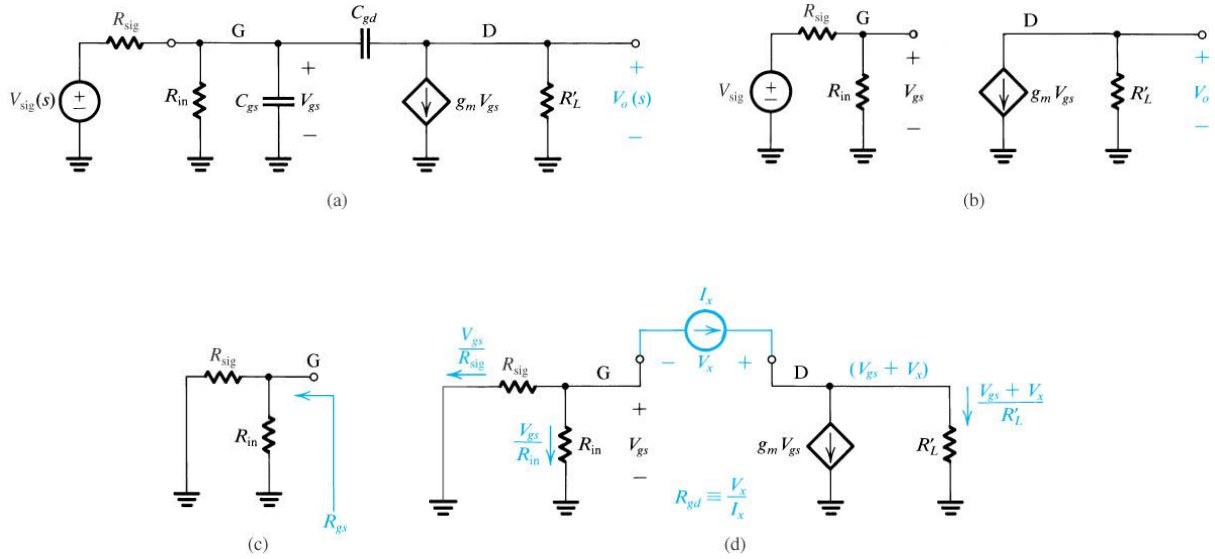
(a)

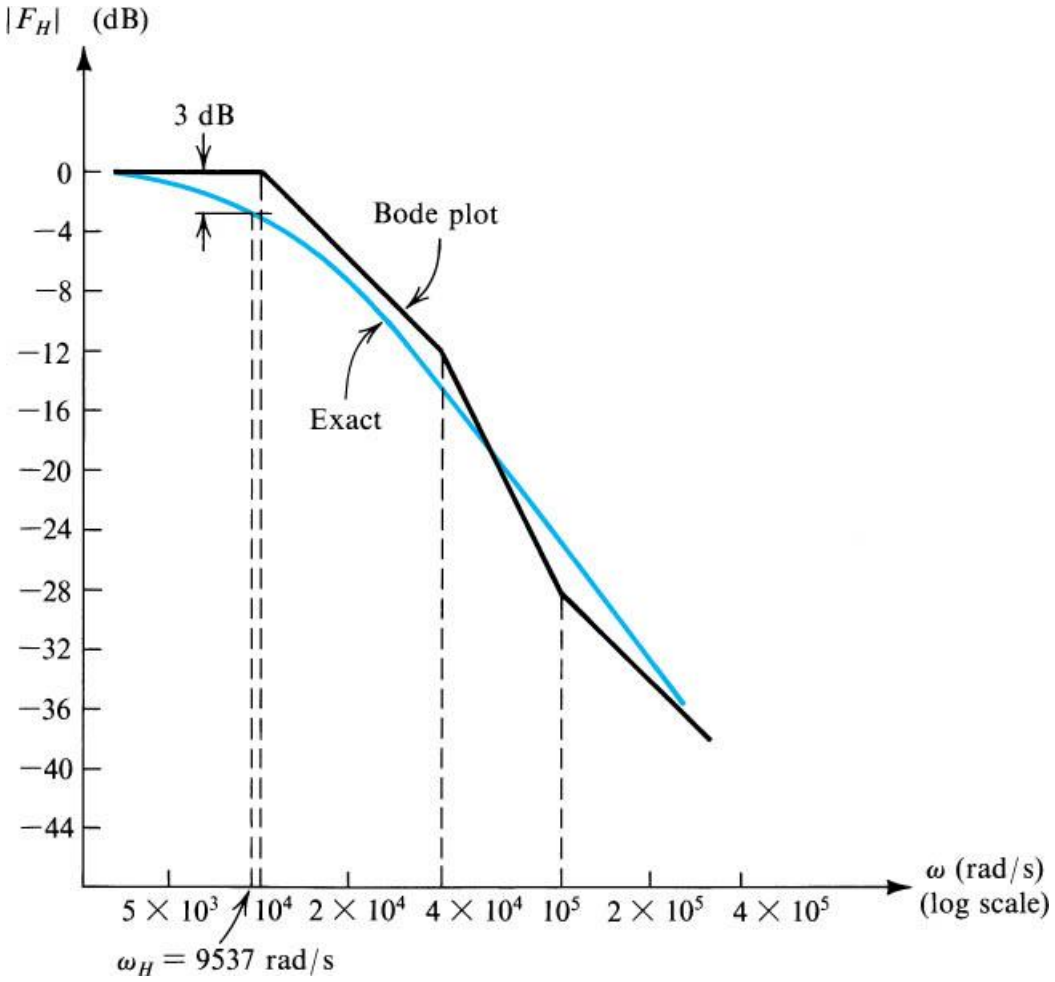


(b)

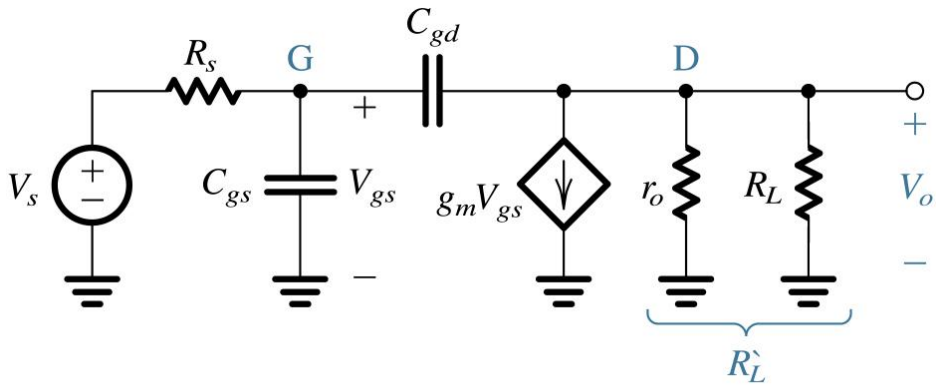
We have seen that a symmetric differential amplifier can be analyzed with a differential half circuit. This still holds true for high-frequency small-signal analysis.

HIGH FREQUENCY ANALYSIS OF MOSFET

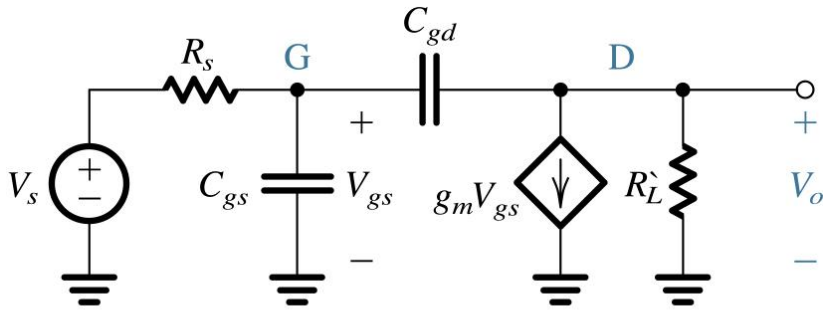




CS Amplifier – High Frequency Response



(a)



(b)

$$\omega_H \cong \frac{1}{\left[C_{gs} + C_{gd}\left(1 + g_m R_L'\right)\right] R_s} = \frac{1}{C_T R_s}$$

SHORT CIRCUIT CURRENT GAIN

In electronics, **gain** is a measure of the ability of a circuit (often an amplifier) to increase the power or amplitude of a signal from the input to the output by adding energy converted from some power supply to the signal. It is usually defined as the mean ratio of the signal output of a system to the signal input of the same system. It is often expressed using the logarithmic decibel (dB) units ("dB gain"). A gain greater than one (zero dB), that is, amplification, is the defining property of an active component or circuit, while a passive circuit will have a gain of less than one.

The term gain alone is ambiguous, and can refer to the ratio of output to input voltage, (voltage gain), current (current gain) or electric power (power gain). In the field of audio and general purpose amplifiers, especially operational amplifiers, the term usually refers to voltage gain, but in radio frequency amplifiers it usually refers to power gain. Furthermore, the term gain is also applied in systems such as sensors where the input and output have different units; in such cases the gain units must be specified, as in "5 microvolts per photon" for the responsivity of a photosensor. The "gain" of a bipolar transistor normally refers to forward current transfer ratio, either h_{FE} ("Beta", the static ratio of I_c divided by I_b at some operating point), or

sometimes h_{fe} (the small-signal current gain, the slope of the graph of I_c against I_b at a point).

The term gain has a slightly different meaning in antenna design; antenna gain is the ratio of power received by a directional antenna to power received by an isotropic antenna.

Power gain

Power gain, in decibels (dB), is defined by the 10 log rule as follows:

$$\text{Gain} = 10 \log \left(\frac{P_{\text{out}}}{P_{\text{in}}} \right) \text{ dB}$$

where P_{in} and P_{out} are the input and output powers respectively.

A similar calculation can be done using a natural logarithm instead of a decimal logarithm, and without the factor of 10, resulting in nepers instead of decibels:

$$\text{Gain} = \ln \left(\frac{P_{\text{out}}}{P_{\text{in}}} \right) \text{ Np}$$

Voltage gain

When power gain is calculated using voltage instead of power, making the substitution ($P=V^2/R$), the formula is:

$$\text{Gain} = 10 \log \frac{\left(\frac{{V_{\text{out}}}^2}{R_{\text{out}}} \right)}{\left(\frac{{V_{\text{in}}}^2}{R_{\text{in}}} \right)} \text{ dB}$$

In many cases, the input and output impedances are equal, so the above equation can be simplified to:

$$\text{Gain} = 10 \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right)^2 \text{ dB}$$

and then the 20 log rule:

$$\text{Gain} = 20 \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right) \text{ dB}$$

This simplified formula is used to calculate a **voltage gain** in decibels, and is equivalent to a power gain only if the impedances at input and output are equal.

Current gain

In the same way, when power gain is calculated using current instead of power, making the substitution ($P = I^2R$), the formula is:

$$\text{Gain} = 10 \log \left(\frac{{I_{\text{out}}}^2 R_{\text{out}}}{{I_{\text{in}}}^2 R_{\text{in}}} \right) \text{ dB}$$

In many cases, the input and output impedances are equal, so the above equation can be simplified to:

$$\text{Gain} = 10 \log \left(\frac{I_{\text{out}}}{I_{\text{in}}} \right)^2 \text{ dB}$$

and then:

$$\text{Gain} = 20 \log \left(\frac{I_{\text{out}}}{I_{\text{in}}} \right) \text{ dB}$$

This simplified formula is used to calculate a **current gain** in decibels, and is equivalent to the power gain only if the impedances at input and output are equal.

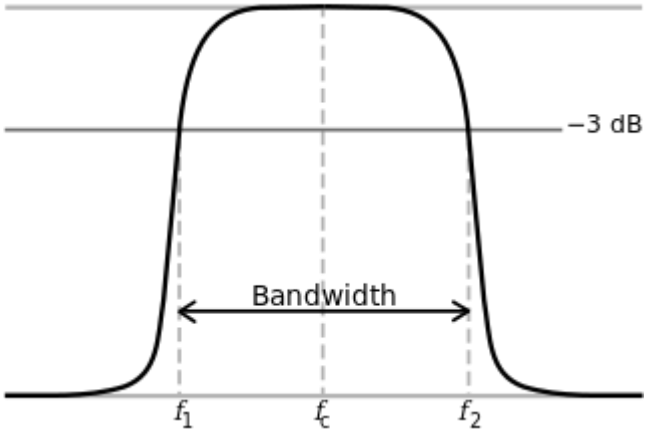
The "current gain" of a bipolar transistor, h_{FE} or h_{fe}, is normally given as a dimensionless number, the ratio of I_c to I_b (or slope of the I_c-versus-I_b graph, for h_{fe}).

In the cases above, gain will be a dimensionless quantity, as it is the ratio of like units (Decibels are not used as units, but rather as a method of indicating a logarithmic relationship). In the bipolar transistor example it is the ratio of the output current to the input current, both measured in Amperes. In the case of other devices, the gain will have a value in SI units. Such is the case with the

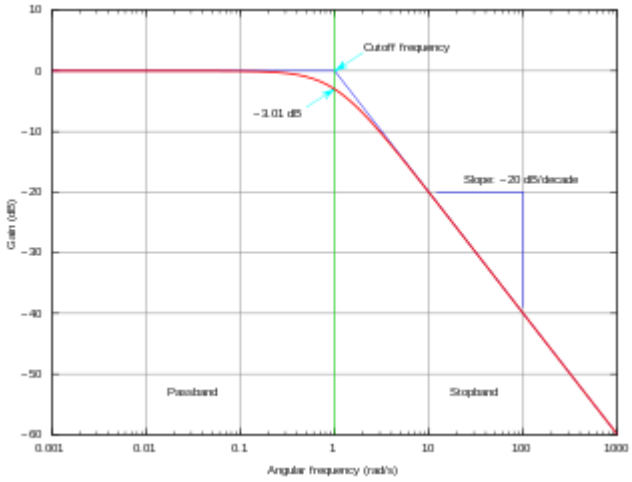
operational transconductance amplifier, which has an open-loop gain (transconductance) in Siemens (mhos), because the gain is a ratio of the output current to the input voltage.

CUT-OFF FREQUENCY

his article is about signal processing. For other uses, see Cutoff (disambiguation).



Magnitude transfer function of a bandpass filter with lower 3 dB cutoff frequency f_1 and upper 3 dB cutoff frequency f_2



A bode plot of the Butterworth filter's frequency response, with corner frequency labeled. (The slope −20 dB per decade also equals −6 dB per octave.)

In physics and electrical engineering, a **cutoff frequency**, **corner frequency**, or **break frequency** is a boundary in a system's frequency

response at which energy flowing through the system begins to be reduced (attenuated or reflected) rather than passing through.

Typically in electronic systems such as filters and communication channels, cutoff frequency applies to an edge in a lowpass, highpass, bandpass, or band-stop characteristic – a frequency characterizing a boundary between a passband and a stopband. It is sometimes taken to be the point in the filter response where a transition band and passband meet, for example, as defined by a 3 dB corner (a frequency for which the output of the circuit is −3 dB of the nominal passband value). Alternatively, a stopband corner frequency may be specified as a point where a transition band and a stopband meet: a frequency for which the attenuation is larger than the required stopband attenuation, which for example may be 30 dB or 100 dB.

In the case of a waveguide or an antenna, the cutoff frequencies correspond to the lower and upper **cutoff wavelengths**.

SINGLE STAGE AMP B.W DETERMINATION

 A **linear** amplifier responds to different frequency components independently, and does not generate harmonic distortion or Intermodulation distortion. No amplifier can provide perfect linearity (even the most linear amplifier has some nonlinearities, since the amplifying devices—transistors or vacuum tubes—follow nonlinear power laws such as square-laws and rely on circuitry techniques to reduce those effects).
 A **nonlinear** amplifier generates significant distortion and so changes the harmonic content; there are situations where this is useful. Amplifier circuits intentionally providing a non-linear transfer function include:

- a device like a Silicon Controlled Rectifier or a transistor used as a switch may be employed to turn either fully ON or OFF a load such as a lamp based on a threshold in a continuously variable input.
- a non-linear amplifier in an analog computer or true RMS converter for example can provide a special transfer function, such as logarithmic or square-law.

- a Class C RF amplifier may be chosen because it can be very efficient, but will be non-linear; following such an amplifier with a "tank" tuned circuit can reduce unwanted harmonics (distortion) sufficiently to be useful in transmitters, or some desired harmonic may be selected by setting the resonant frequency of the tuned circuit to a higher frequency rather than fundamental frequency in frequency multiplier circuits.
- Automatic gain control circuits require an amplifier's gain be controlled by the time-averaged amplitude so that the output amplitude varies little when weak stations are being received. The non-linearities are assumed to be arranged so the relatively small signal amplitude suffers from little distortion (cross-channel interference or intermodulation) yet is still modulated by the relatively large gain-control DC voltage.
- AM detector circuits that use amplification such as Anode-bend detectors, Precision rectifiers and Infinite impedance detectors (so excluding unamplified detectors such as Cat's-whisker detectors), as well as peak detector circuits, rely on changes in amplification based on the signal's instantaneous amplitude to derive a direct current from an alternating current input.
- Operational amplifier comparator and detector circuits.

 A **wideband** amplifier has a precise amplification factor over a wide frequency range, and is often used to boost signals for relay in communications systems. A **narrowband** amp amplifies a specific narrow range of frequencies, to the exclusion of other frequencies.
 An **RF** amplifier amplifies signals in the radio frequency range of the electromagnetic spectrum, and is often used to increase the sensitivity of a receiver or the output power of a transmitter.[7]
 An **audio amplifier** amplifies audio frequencies. This category subdivides into small signal amplification, and power amps that are optimised to driving speakers, sometimes with multiple amps grouped together as separate or bridgeable channels to accommodate different audio reproduction requirements. Frequently used terms within audio amplifiers include:

- Preamplifier (preamp), which may include a phono preamp with RIAA equalization, or tape head preamps with CCIR

equalisation filters. They may include filters or tone control circuitry.
- Power amplifier (normally drives loudspeakers), headphone amplifiers, and public address amplifiers.
- Stereo amplifiers imply two channels of output (left and right), though the term simply means "solid" sound (referring to three-dimensional)—so quadraphonic stereo was used for amplifiers with four channels. 5.1 and 7.1 systems refer to Home theatre systems with 5 or 7 normal spacial channels, plus a subwoofer channel.

MULTI STAGE AMP B.W DETERMINATION

The performance obtainable from a single stage amplifier is often insufficient for many applications, hence several stages may be combined forming a **multistage amplifier**. These stages are connected in cascade, i.e. output of the first stage is connected to form input of second stage, whose output becomes input of third stage, and so on.

Overall gain

The overall gain of a multistage amplifier is the product of the gains of the individual stages (ignoring potential loading effects):

$$\text{Gain (A)} = A_1 * A_2 * A_3 * A_4 * \ldots * A_n.$$

Alternately, if the gain of each amplifier stage is expressed in decibels (dB), the total gain is the sum of the gains of the individual stages:

$$\text{Gain in dB (A)} = A_1 + A_2 + A_3 + A_4 + \ldots A_n$$

Inter-stage coupling

Depending on the manner in which the different amplifier stages are connected, one of the following amplifiers may result:

- R-C coupled amplifier
- R-L coupled amplifier

- L-C coupled amplifier
- Transformer coupled amplifier
- Direct coupled amplifier

UNIT-5 IC MOSFET AMPLIFIERS

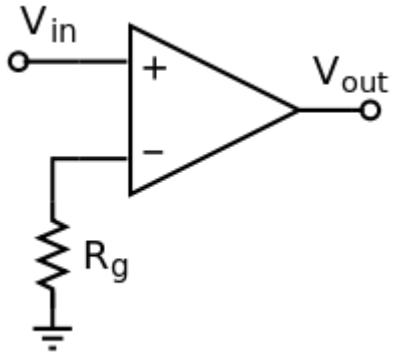
An **operational amplifier** (op-amp) is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output.[1] In this configuration, an op-amp produces an output potential (relative to circuit ground) that is typically hundreds of thousands of times larger than the potential difference between its input terminals.[2]

Operational amplifiers had their origins in analog computers, where they were used to do mathematical operations in many linear, non-linear and frequency-dependent circuits. Characteristics of a circuit using an op-amp are set by external components with little dependence on temperature changes or manufacturing variations in the op-amp itself, which makes op-amps popular building blocks for circuit design.

Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Many standard IC op-amps cost only a few cents in moderate production volume; however some integrated or hybrid operational amplifiers with special performance specifications may cost over $100 US in small quantities.[3] Op-amps may be packaged as components, or used as elements of more complex integrated circuits.

The op-amp is one type of differential amplifier. Other types of differential amplifier include the fully differential amplifier (similar to the op-amp, but with two outputs), the instrumentation amplifier (usually built from three op-amps), the isolation amplifier (similar to the instrumentation amplifier, but with tolerance to common-mode voltages that would destroy an ordinary op-amp), and negative feedback amplifier (usually built from one or more op-amps and a resistive feedback network).

Operation



An op-amp without negative feedback (a comparator)

The amplifier's differential inputs consist of a non-inverting input (+) with voltage V_+ and an inverting input (–) with voltage $V_–$; ideally the op-amp amplifies only the difference in voltage between the two, which is called the differential input voltage. The output voltage of the op-amp V_{out} is given by the equation:

$$V_{\text{out}} = A_{\text{OL}} (V_+ - V_-)$$

where A_{OL} is the open-loop gain of the amplifier (the term "open-loop" refers to the absence of a feedback loop from the output to the input).

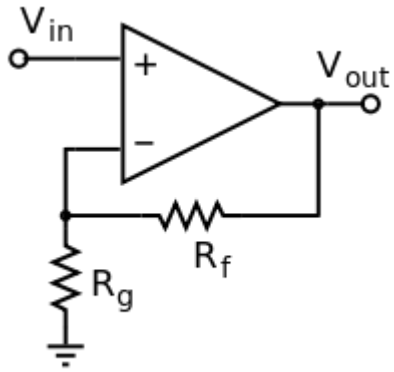
Open loop

The magnitude of A_{OL} is typically very large—100,000 or more for integrated circuit op-amps—and therefore even a quite small difference between V_+ and $V_–$ drives the amplifier output nearly to the supply voltage. Situations in which the output voltage is equal to or greater than the supply voltage are referred to as saturation of the amplifier. The magnitude of A_{OL} is not well controlled by the manufacturing process, and so it is impractical to use an operational amplifier as a stand-alone differential amplifier.

Without negative feedback, and perhaps with positive feedback for regeneration, an op-amp acts as a comparator. If the inverting input is

held at ground (0 V) directly or by a resistor R_g, and the input voltage V_{in} applied to the non-inverting input is positive, the output will be maximum positive; if V_{in} is negative, the output will be maximum negative. Since there is no feedback from the output to either input, this is an open loop circuit acting as a comparator. The circuit's gain is just the A_{OL} of the op-amp.

Closed loop



An op-amp with negative feedback (a non-inverting amplifier)

If predictable operation is desired, negative feedback is used, by applying a portion of the output voltage to the inverting input. The closed loop feedback greatly reduces the gain of the circuit. When negative feedback is used, the circuit's overall gain and response becomes determined mostly by the feedback network, rather than by the op-amp characteristics. If the feedback network is made of components with values small relative to the op amp's input impedance, the value of the op-amp's open loop response A_{OL} does not seriously affect the circuit's performance. The response of the op-amp circuit with its input, output, and feedback circuits to an input is characterized mathematically by a transfer function; designing an op-amp circuit to have a desired transfer function is in the realm of electrical engineering. The transfer functions are important in most applications of op-amps, such as in analog computers. High input impedance at the input terminals and low output impedance at the output terminal(s) are particularly useful features of an op-amp.

In the non-inverting amplifier on the right, the presence of negative feedback via the voltage divider R_f, R_g determines the closed-loop gain $A_{CL} = V_{out} / V_{in}$. Equilibrium will be established when V_{out} is just sufficient to "reach around and pull" the inverting input to the same voltage as V_{in}. The voltage gain of the entire circuit is thus $1 + R_f/R_g$. As a simple example, if V_{in} = 1 V and $R_f = R_g$, V_{out} will be 2 V, exactly the amount required to keep V_- at 1 V. Because of the feedback provided by the R_f, R_g network, this is a closed loop circuit.

Another way to analyze this circuit proceeds by making the following (usually valid) assumptions:[4]

- When an op-amp operates in linear (i.e., not saturated) mode, the difference in voltage between the non-inverting (+) pin and the inverting (−) pin is negligibly small.
- The input impedance between (+) and (−) pins is much larger than other resistances in the circuit.

The input signal V_{in} appears at both (+) and (−) pins, resulting in a current i through R_g equal to V_{in}/R_g.

$$i = \frac{V_{\text{in}}}{R_g}$$

Since Kirchhoff's current law states that the same current must leave a node as enter it, and since the impedance into the (−) pin is near infinity, we can assume practically all of the same current i flows through R_f, creating an output voltage

$$V_{\text{out}} = V_{\text{in}} + i \times R_f = V_{\text{in}} + \left(\frac{V_{\text{in}}}{R_g} \times R_f\right) = V_{\text{in}} + \frac{V_{\text{in}} \times R_f}{R_g} = V_{\text{in}}\left(1 + \frac{R_f}{R_g}\right)$$

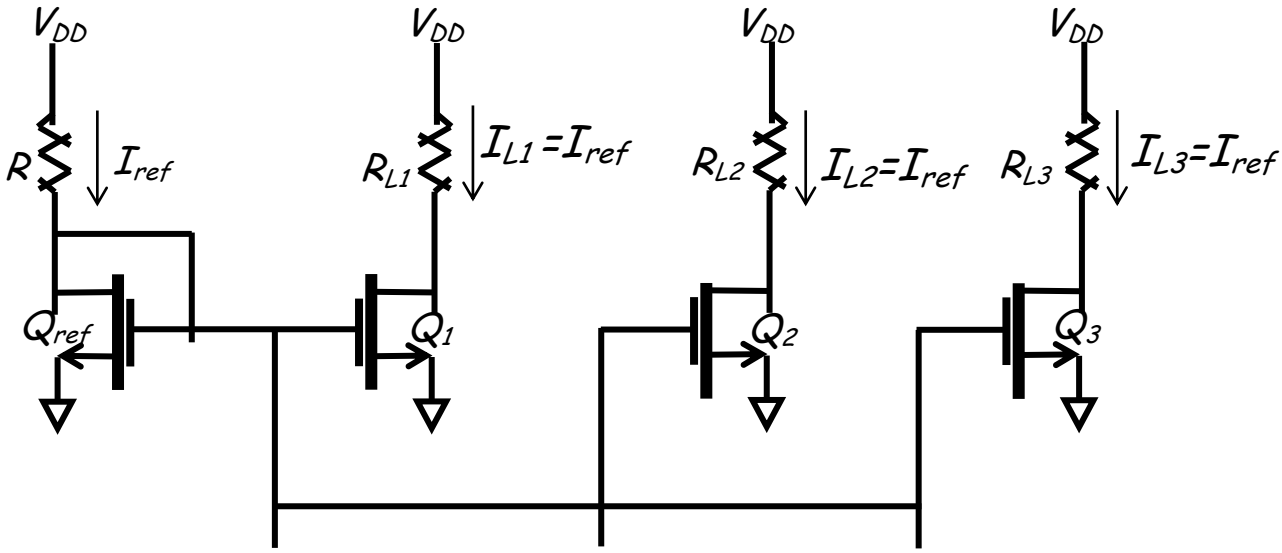
By combining terms, we determine the closed-loop gain A_{CL}:

$$A_{\text{CL}} = \frac{V_{\text{out}}}{V_{\text{in}}} = 1 + \frac{R_f}{R_g}$$

IC biasing Current steering circuit using MOSFET

Current Steering Circuits

A current mirror may consist of **many** MOSFET current sources!



This circuit is particularly useful in integrated circuit design, where **one** resistor R is used to make **multiple** current sources.

Q: What if we want to make the sources have **different** current values? Do we need to make **additional** current mirrors?

A: NO!!

Recall that the current mirror simply ensures that the gate to source voltages of **each** transistor is **equal** to the gate to source voltage of the **reference**:

$$V_{GS}^{ref} = V_{GS1} = V_{GS2} = V_{GS3} = \cdots$$

Therefore, **if** each transistor is identical (i.e., $K_{ref} = K_1 = \cdots$, and $V_t^{ref} = V_{t1} = V_{t2} = \cdots$) then:

$$\begin{aligned} I_{ref} &= K_{ref}\left(V_{GS}^{ref} - V_t^{ref}\right)^2 \\ &= K_n\left(V_{GSn} - V_{tn}\right)^2 = I_{Dn} \end{aligned}$$

In other words, **if** each transistor Q_n is **identical** to Q_{ref}, then each current I_{Dn} will **equal** reference current I_{ref}.

But, consider what happens if the MOSFETS are not identical. Specifically, consider the case where $K_n \neq K_{ref}$ (but $V_{tn} = V_t^{ref}$).

Remember, we know that $V_{GSn} = V_{GS}^{ref}$ still, even when $K_n \neq K_{ref}$. Thus, the drain current I_{Dn} will now be:

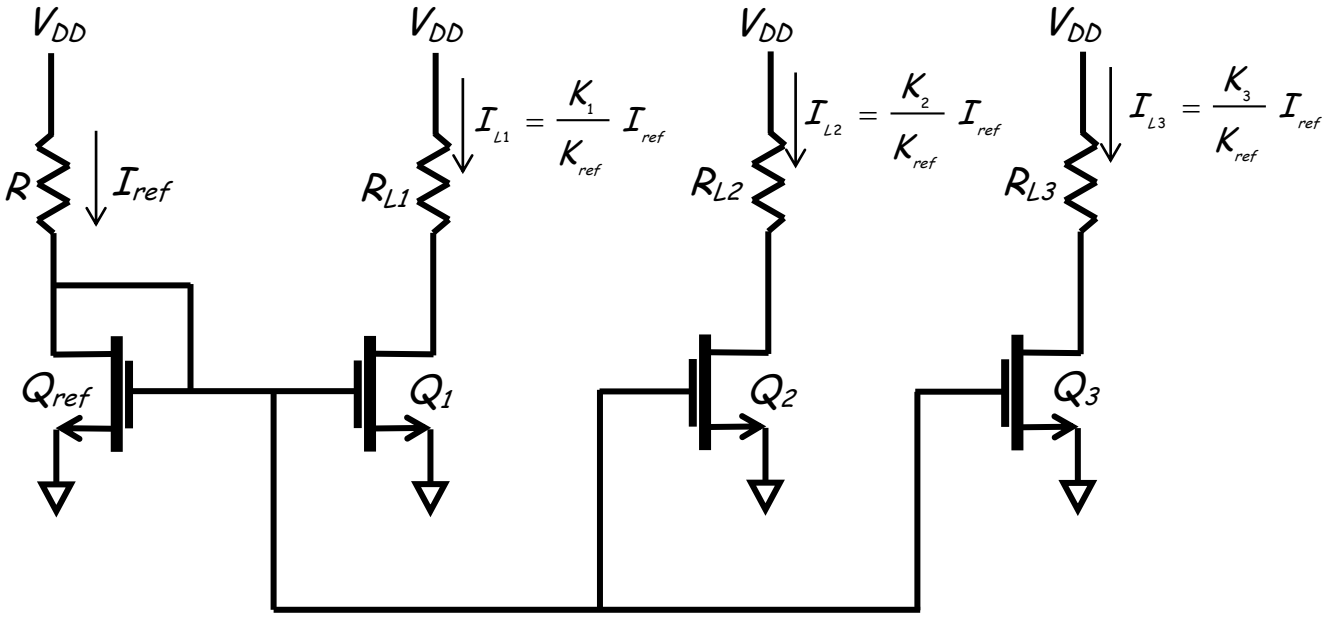
$$\begin{aligned} I_{Dn} &= K_n\left(V_{GSn} - V_{tn}\right)^2 \\ &= K_n\left(V_{GS}^{ref} - V_t^{ref}\right)^2 \\ &= K_n\left(\frac{I_{ref}}{K_{ref}}\right) \\ &= \left(\frac{K_n}{K_{ref}}\right) I_{ref} \end{aligned}$$

The drain current is a scaled value of I_{ref}!

For example, if K_1 is twice that of K_{ref} (i.e., $K_1 = 2K_{ref}$), then I_{D1} will be twice as large as I_{ref} (i.e., $I_1 = 2I_{ref}$).

From the standpoint of integrated circuit design, we can change the value of K by modifying the MOSFET channel **width-to-length ratio** (W/L) for each transistor.

$$\frac{K_n}{K_{ref}} = \frac{\frac{1}{2}k'\left(W/L\right)_n}{\frac{1}{2}k'\left(W/L\right)_{ref}} = \frac{\left(W/L\right)_n}{\left(W/L\right)_{ref}}$$

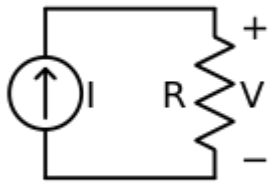


MOSFET current sources

A **current source** is an electronic circuit that delivers or absorbs an electric current which is independent of the voltage across it.

A current source is the dual of a voltage source. The term constant-current 'sink' is sometimes used for sources fed from a negative voltage supply. Figure 1 shows the schematic symbol for an ideal

current source, driving a resistor load. There are two types - an **independent current source** (or sink) delivers a constant current. A **dependent current source** delivers a current which is proportional to some other voltage or current in the circuit.



PMOS and NMOS current sources

P-type metal-oxide-semiconductor logic uses p-channel metal-oxide-semiconductor field effect transistors (MOSFETs) to implement logic gates and other digital circuits. PMOS transistors operate by creating an inversion layer in an n-type transistor body. This inversion layer, called p-channel, can conduct holes between p-type "source" and "drain" terminals.

The p-channel is created by applying voltage to the third terminal called gate. Like other MOSFETs, PMOS transistors have four modes of operation: cut-off (or subthreshold), triode, saturation (sometimes called active), and velocity saturation.

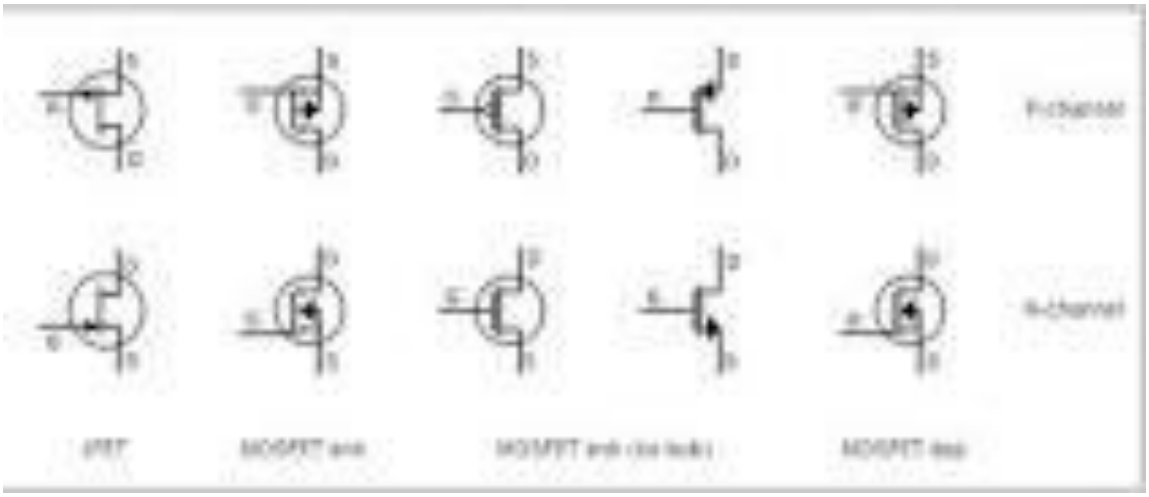
The p-type MOSFETs are arranged in a so-called "pull-up network" (PUN) between the logic gate output and positive supply voltage, while a resistor is placed between the logic gate output and the negative supply voltage. The circuit is designed such that if the desired output is high, then the PUN will be active, creating a current path between the positive supply and the output.

While PMOS logic is easy to design and manufacture (a MOSFET can be made to operate as a resistor, so the whole circuit can be made with PMOS FETs), it has several shortcomings as well. The worst problem is that a DC current flows through a PMOS logic gate when the PUN is active, that is whenever the output is high. This leads to static power dissipation even when the circuit sits idle.

Also, PMOS circuits are slow to transition from high to low. When transitioning from low to high, the transistors provide low resistance, and the capacitative charge at the output accumulates very quickly (similar to charging a capacitor through a very low resistor). But the resistance between the output and the negative supply rail is much greater, so the high to low transition takes longer (similar to discharge a capacitor through a high resistor value). Using a resistor of lower value will speed up the process but also increases static power dissipation.

Additionally, the asymmetric input logic levels make PMOS circuits susceptible to noise.

Though initially easier to manufacture, PMOS logic was later supplanted by NMOS logic because NMOS is faster than PMOS. Modern fabs use CMOS, which uses both PMOS and NMOS transistors together. Static CMOS logic leverages the advantages of both by using NMOS and PMOS together in the wafer.



Amplifier with active loads - enhancement load, Depletion load

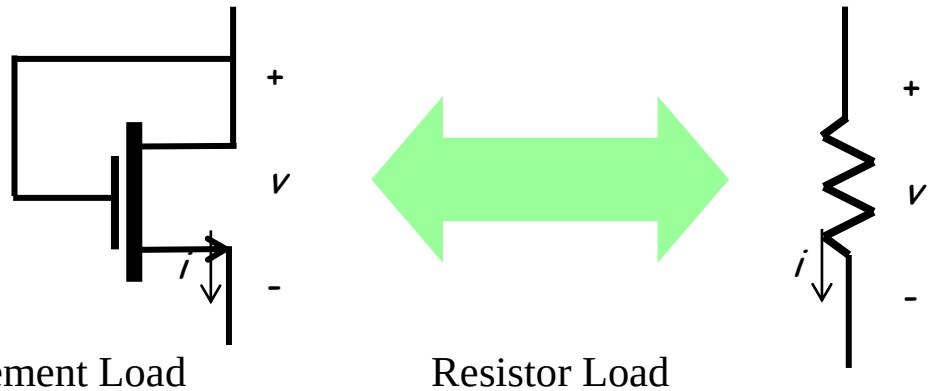
Enhancement Loads

Resistors take up far too much **space** on integrated circuit substrates.

Therefore, we need to make a **resistor** out of a **transistor**!

Q: How can we do that!? After all, a resistor is a **two** terminal device, whereas a transistor is a **three** terminal device.

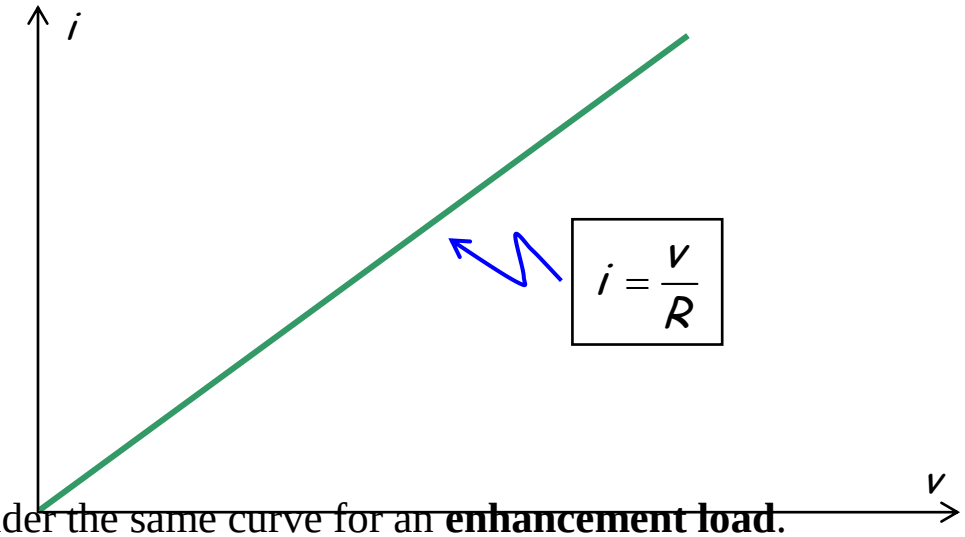
A: We can make a two terminal device from a MOSFET by **connecting** the gate and the drain!



Enhancement Load Resistor Load

Q: How does this "**enhancement load**" resemble a resistor?

A: Consider the i-v curve for a **resistor**:



Now consider the same curve for an **enhancement load**.

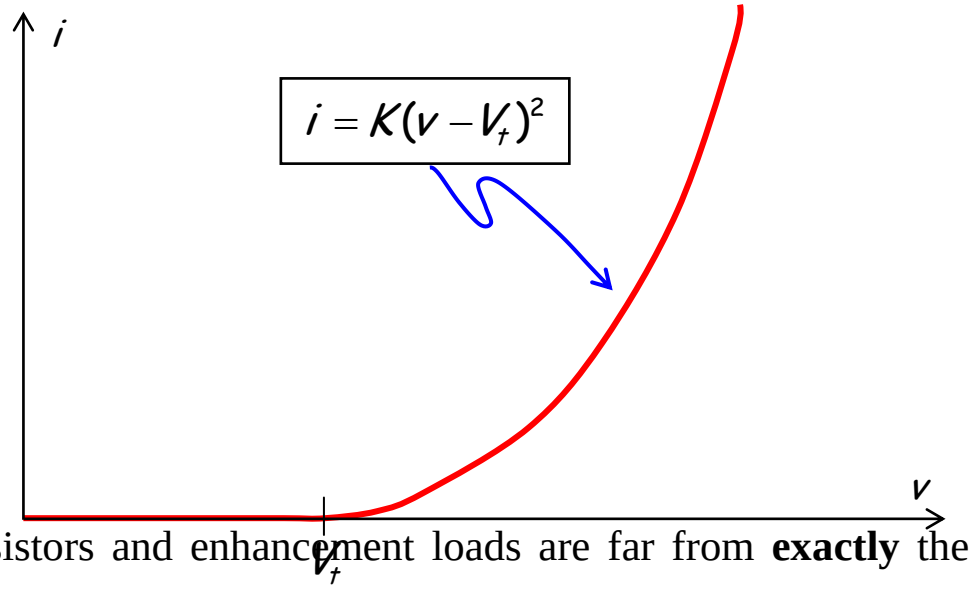
Since the gate is tied to the drain, we find $v_G = v_D$, and thus $v_{GS} = v_{DS}$. As a result, we find that $v_{DS} > v_{GS} - V_t$ **always**.

Therefore, we find that if $v_{GS} > V_t$, the MOSFET will be in **saturation** ($i_D = K(v_{GS} - V_t)^2$), whereas if $v_{GS} < V_t$, the MOSFET is in **cutoff** ($i_D = 0$).

Since for enhancement load $i = i_D$ and $v = v_{GS}$, we can describe the enhancement load as:

$$i = \begin{cases} 0 & \text{for } v < V_t \\ K(v - V_t)^2 & \text{for } v > V_t \end{cases}$$

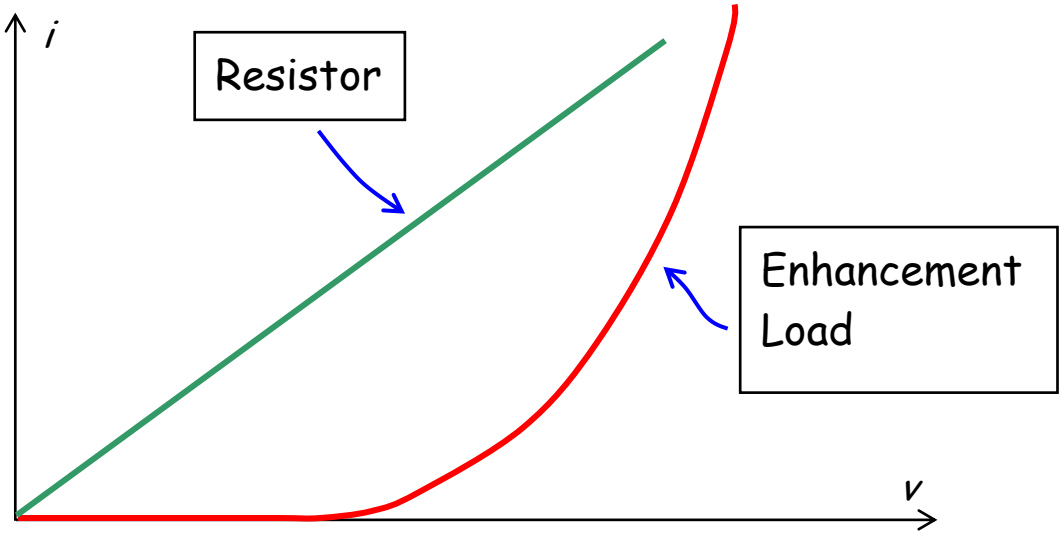
Plotting this equation:



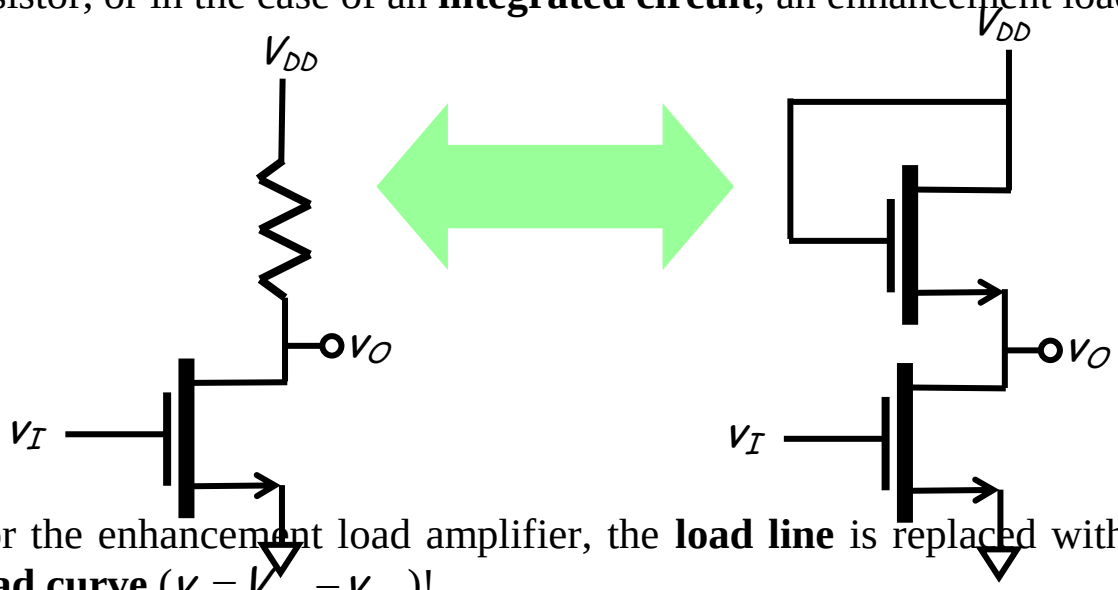
So, resistors and enhancement loads are far from **exactly** the same, but:

1) They **both** have $i = 0$ when $v = 0$.

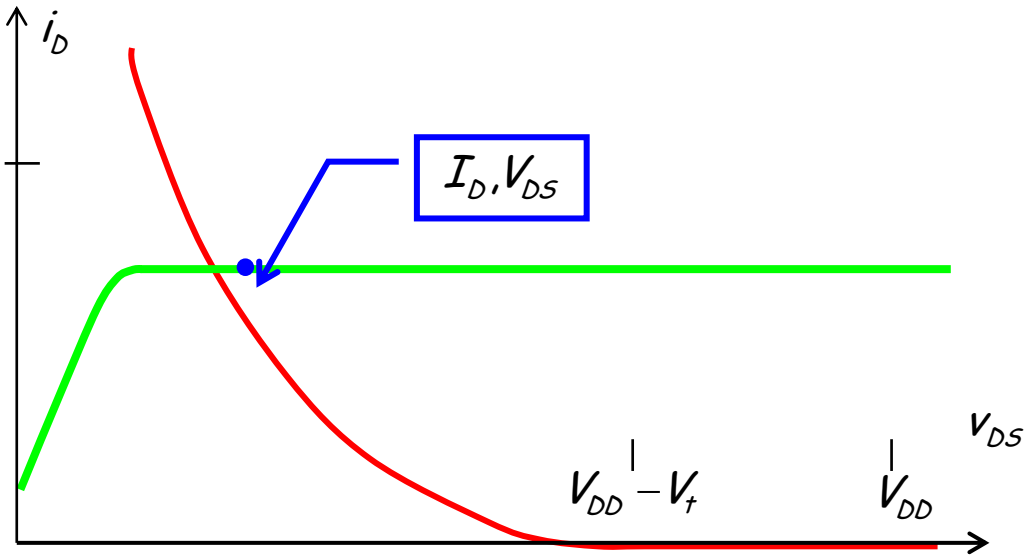
2) They **both** have increasing current i with increasing voltage v.



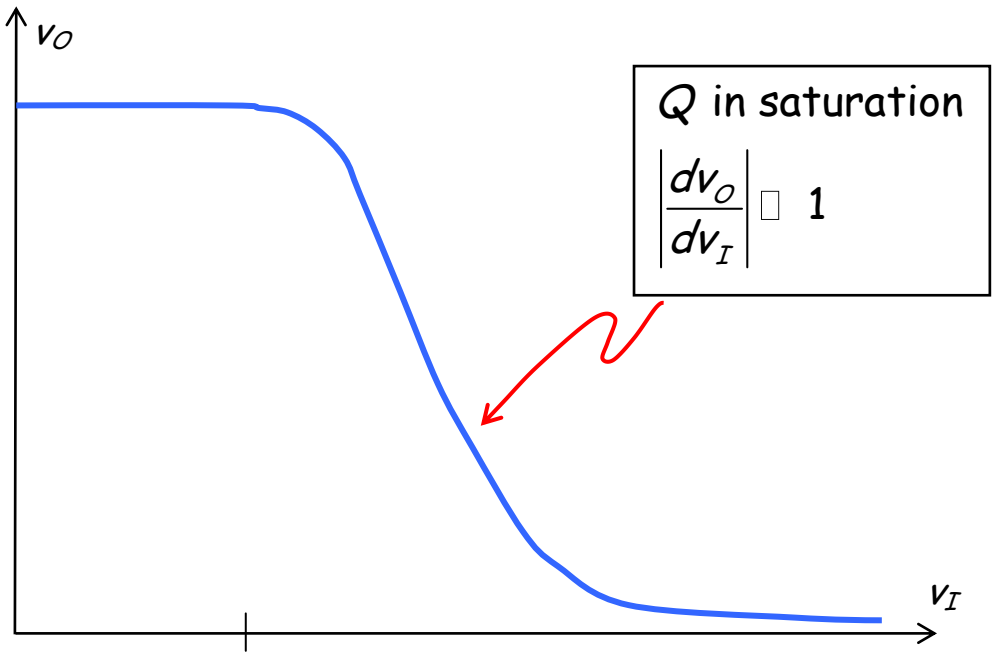
Therefore, we can build a **common source** amplifier with either a resistor, or in the case of an **integrated circuit**, an enhancement load.



For the enhancement load amplifier, the **load line** is replaced with a **load curve** ($v = V_{DD} - v_{DS}$)!



And the **transfer function** of this circuit is:



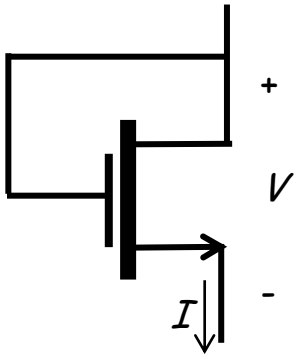
Q: What is the **small-signal** behavior of an enhancement load?

A: The enhancement load is made of a MOSFET device, and we **understand** the small-signal behavior for a MOSFET!

Step 1 - DC Analysis

If $V > V_t$, then $I = K(V - V_t)^2$ or:

$$V = \sqrt{\frac{I}{K}} + V_t$$



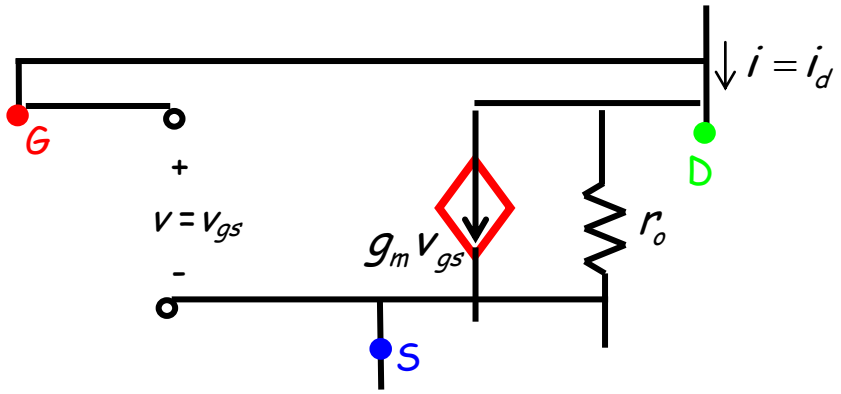
Step 2 – Determine gm and ro

$$g_m = 2K\left(V_{GS} - V_t\right) = 2K\left(V - V_t\right)$$

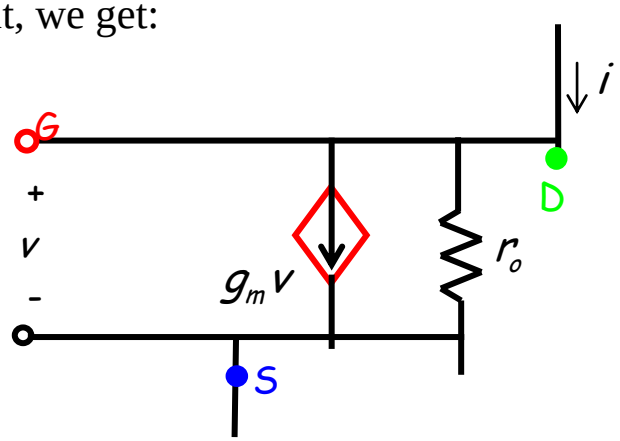
$$r_o = \frac{1}{\lambda I_D} = \frac{1}{\lambda I} = \frac{1}{\lambda K\left(V - V_t\right)^2}$$

Step 3 – Determine the small-signal circuit

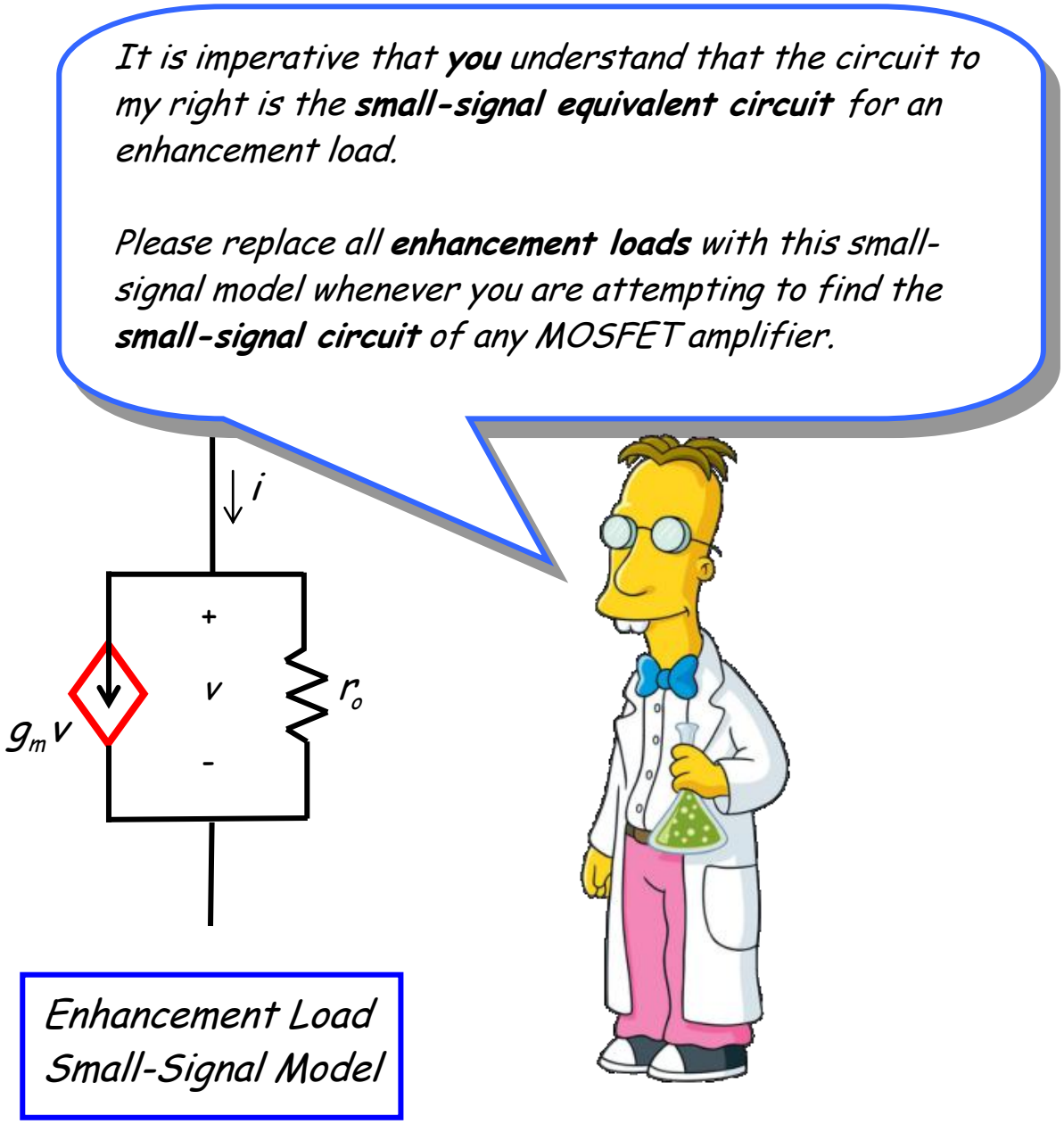
Inserting the MOSFET **small-signal model**, we get:



Redrawing this circuit, we get:

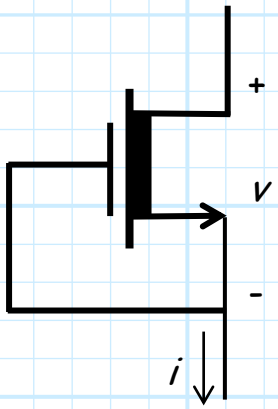


Or, simplifying further, we have the small-signal equivalent circuit for an enhancement load:



Depletion Loads

We can also make a transistor "load" by using a **depletion** MOSFET!



Note $v_G = v_s$, therefore $v_{GS} = 0$!

Q: Doesn't that mean that the MOSFET is in **cutoff**!?

A: No! Note we are using a **depletion** MOSFET. Recall that for these devices, a conducting channel is **implanted**—we do not need to **induce** a channel!

Instead, the channel is cutoff only if it is fully depleted, where depletion is accomplished by making the gate-to-source voltage **negative** (for NMOS). Thus, the threshold voltage for a depletion NMOS transistor is negative ($V_t < 0$).

For the depletion load shown above, $V_{GS} = 0 > V_t$, so that the MOSFET can **never** be in cutoff—the channel is always conducting!

The question then is whether the MOSFET is in **triode** or **saturation**. Recall an n-channel MOSFET is in triode **if**:

$$v_{DS} < v_{GS} - V_t$$

and since $v = v_{DS}$ and $v_{GS} = 0$, we find that the depletion load MOSFET is in **triode** if:

$$v < -V_t$$

Note that since the threshold voltage for a **depletion** NMOS device is negative, the value $-V_t$ is a **positive** number!

Recall that a MOSFET in **triode** has drain current:

$$i_D = K\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right]$$

And since for the **depletion load**, $i = i_D$, $v = v_{DS}$ and $v_{GS} = 0$:

$$\begin{aligned} i &= K\left[-2V_t\, v - v^2\right] \\ &= -K(2V_t + v)v \end{aligned}$$

Since $v < -V_t$, this current value is actually **positive** $(i > 0)$ if voltage v is positive.

Now, if $v > -V_t$ (i.e., $v_{DS} > v_{GS} - V_t$), we find that the depletion MOSFET in the load will be in **saturation**, and thus $i_D = K(v_{GS} - V_t)^2$. Since for the **depletion load** $i = i_D$, $v = v_{DS}$ and $v_{GS} = 0$, we find that in **saturation**:

$$i = K V_t^2$$

A **constant**!

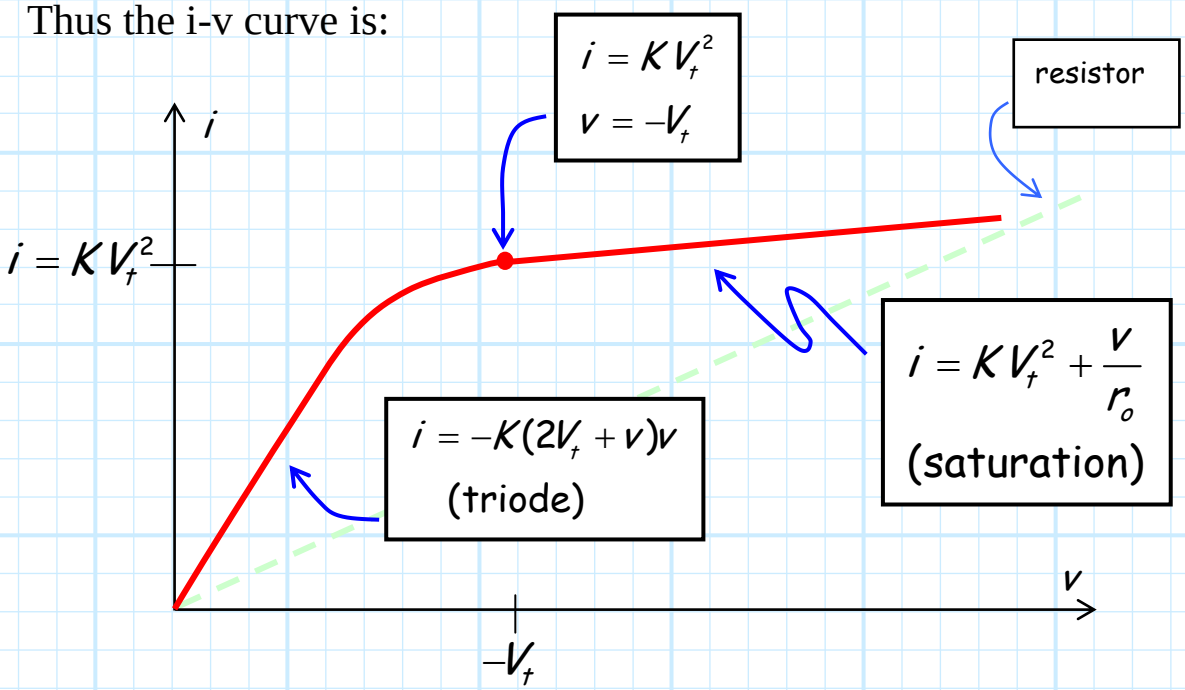
If we account for **channel-length modulation** effects (i.e., the MOSFET output resistance), we modify the above equation to be:

$$i = K V_t^2 + \frac{v}{r_o}$$

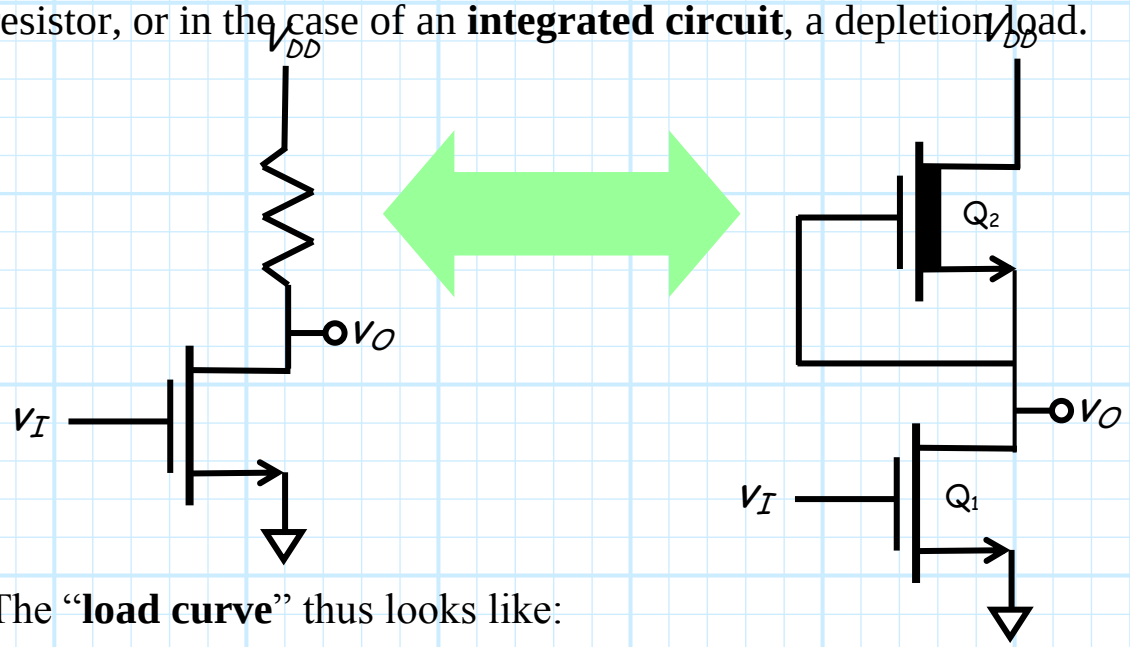
Summarizing, we find that the i-v relationship for a **depletion load** is:

$$i = \begin{cases} -K(2V_t + v)v & \text{for } v < -V_t \\ K V_t^2 + \dfrac{v}{r_o} & \text{for } v > -V_t \end{cases}$$

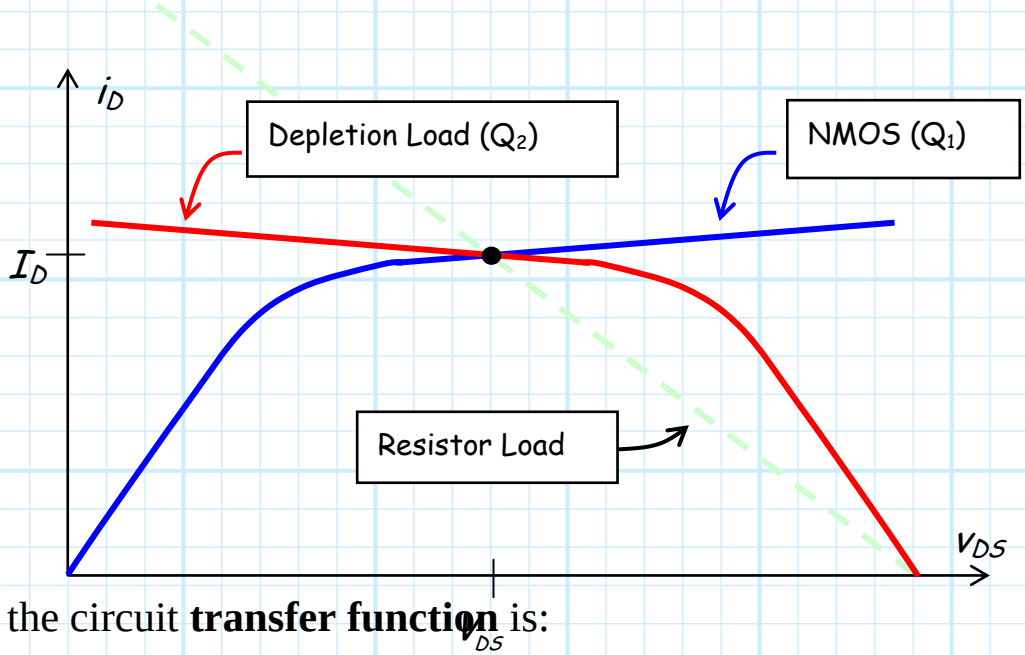
Thus the i-v curve is:



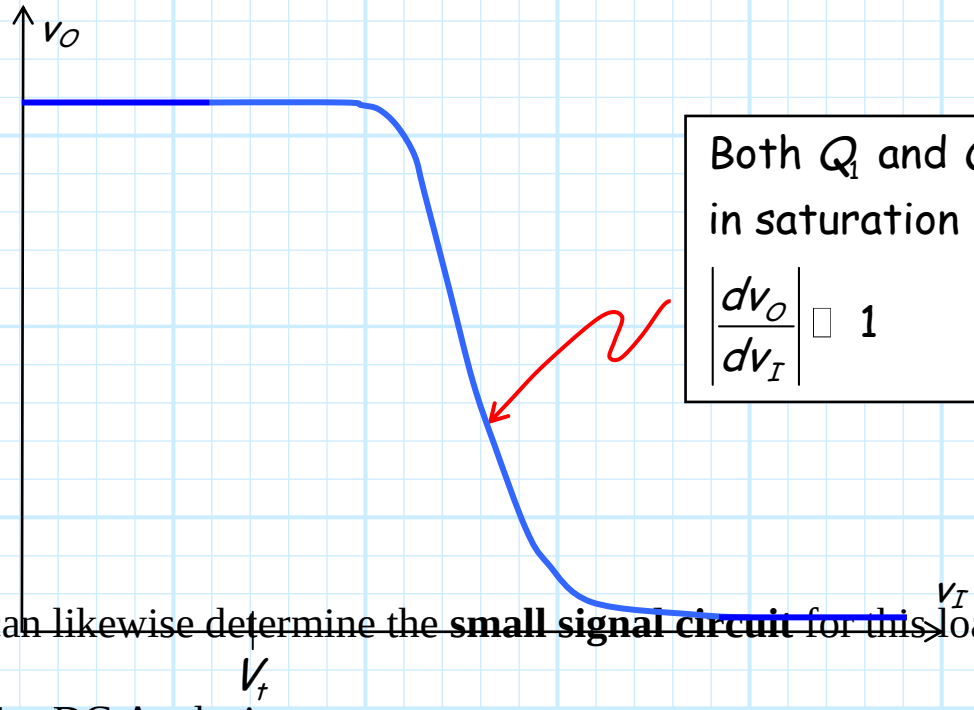
Therefore, we can build a **common source** amplifier with either a resistor, or in the case of an **integrated circuit**, a depletion load.



The "**load curve**" thus looks like:



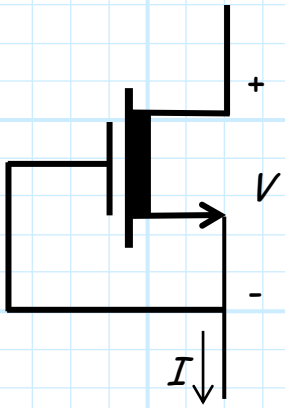
And the circuit **transfer function** is:



We can likewise determine the **small signal circuit** for this load.

Step1 – DC Analysis

In saturation:



$$I = KV_t^2$$

and:

$$V_{GS} = 0$$

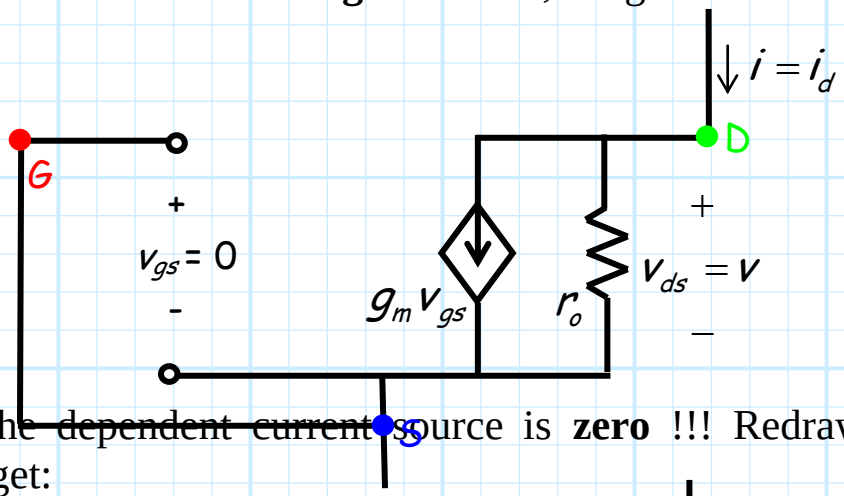
Step 2 – Determine Small-signal Parameters

$$g_m = -2KV_t \quad \Leftarrow \quad \text{a positive number!}$$

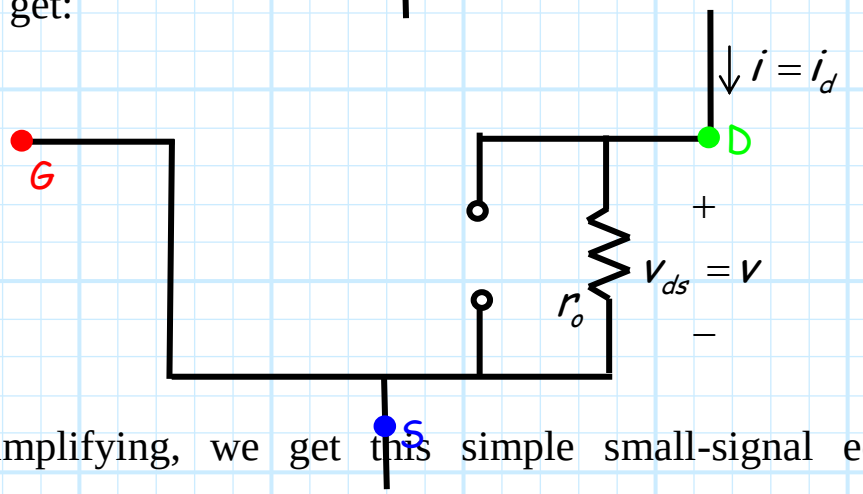
$$r_o = \frac{1}{\lambda I} = \frac{1}{\lambda K V_t^2}$$

Steps 3 & 4 – Small-Signal Analysis

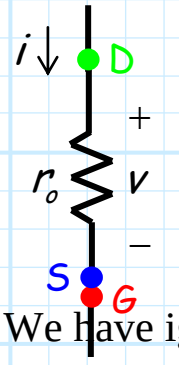
Inserting the MOSFET **small-signal model**, we get:



Note that the dependent current source is **zero** !!! Redrawing this circuit, we get:



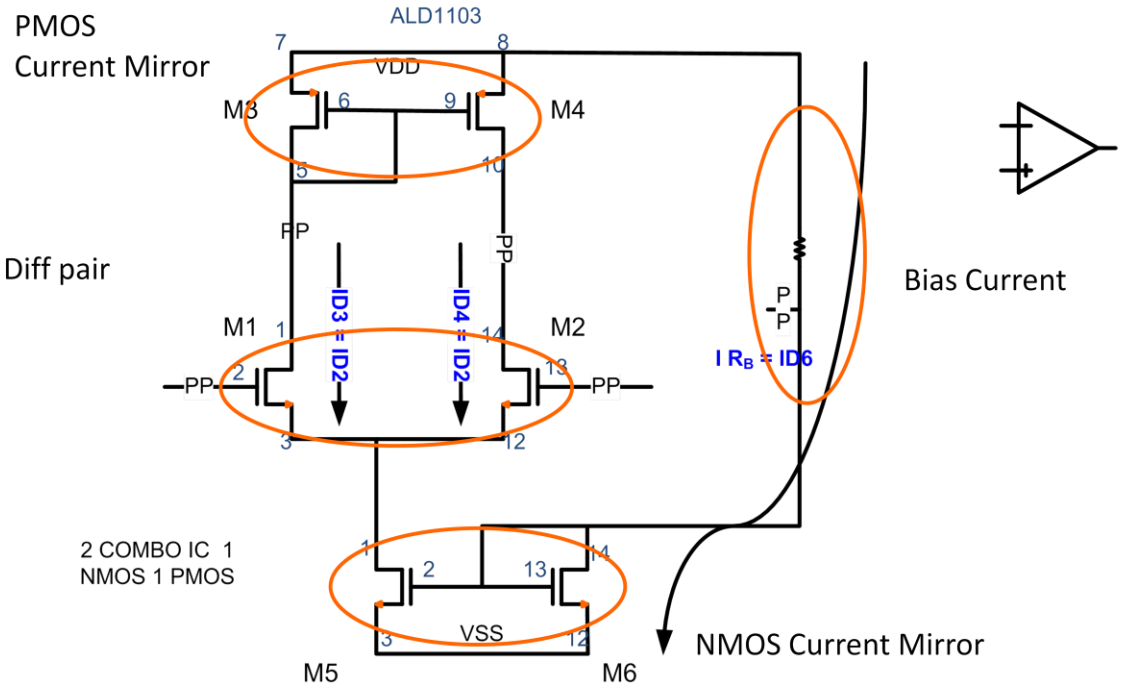
Further simplifying, we get this simple small-signal equivalent circuit:



The Depletion Load Small-Signal Model

WARNING!: We have ignored **body effects**!

Diff Amp



SPICE Models:

NMOS LEVEL=2 +VTO=-0.7 KP=5000E-6 LAMBDA=0.02 GAMMA=0.45 +TOX=90E-9 NSUB=3.7E15
PMOS LEVEL=2 +VTO=0.7 KP=400E-6 LAMBDA=0.05 GAMMA=0.9 +TOX=90E-9 NSUB=3.7E15

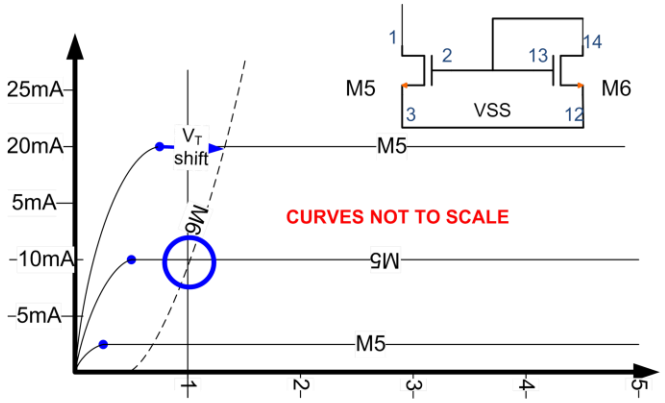
Note

;

Current Mirroring (Copy)

;

Square Law Operation– $I_D = \frac{\beta(V_{GS} - V_{T0})^2}{2}$ $V_{GSN} = \sqrt{\frac{2I_D\beta}{\beta n}} + V_{T0N}$

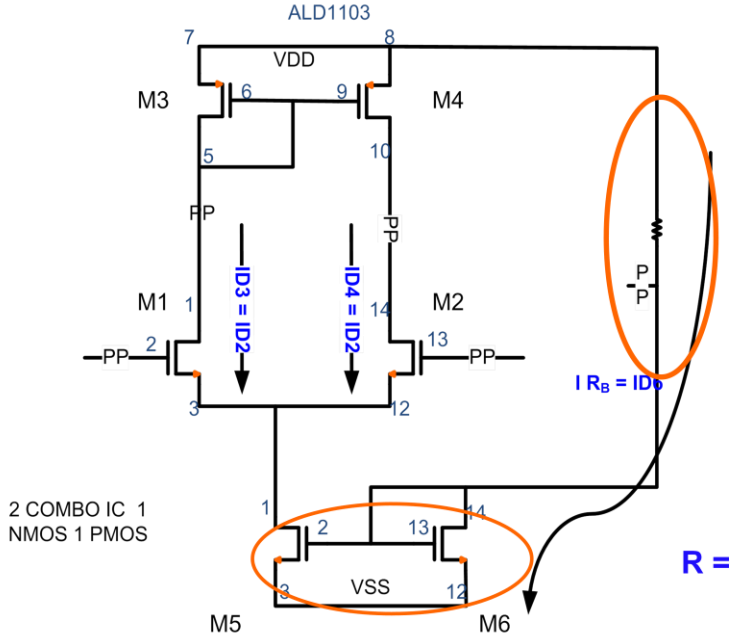


Observations

$V_{GS1} = V_{GS2}, \quad \beta_5 = \beta_6 \quad V_{T5} = V_{T6}; \quad And \quad from \quad V_{GSN} = \sqrt{\frac{2I_D\beta}{\beta n}} + V_{T0N}$

$$\sqrt{\frac{2I_{D5}\beta}{\beta n}} + V_{T0N} = \sqrt{\frac{2I_{D6}\beta}{\beta n}} + V_{T0N} = I_{D5} = I_{D6}$$

Developing the Bias Current



Setting biasing Current of Diff Amp, Note:

- **$I_R = I_{D6}$**
- **$V_{DD} - V_{SS} = V_{SG} + I_B R_B$;**
- $V_{GSN} = \sqrt{\frac{2I_D\beta}{\beta n}} - V_{T0N}$

R = (√ß·2VDD - VTN) - √(2·I))/(I·√ß)